

PG600-B02 NI GHTHAWK

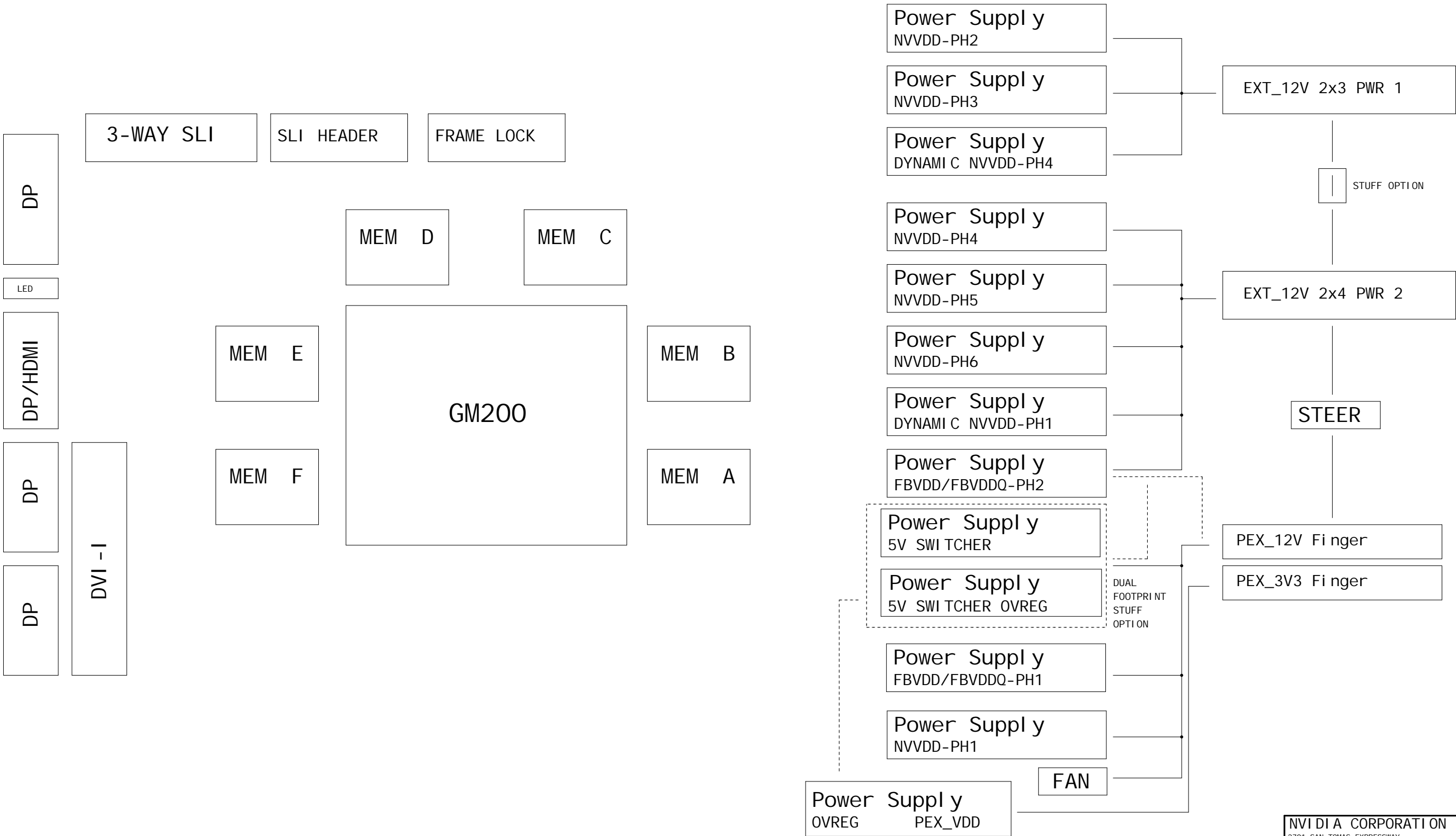
GB3B-384, 6GB GDDR5 128Mx32

DP + HDMI /DP + DP + DP + DVI -I

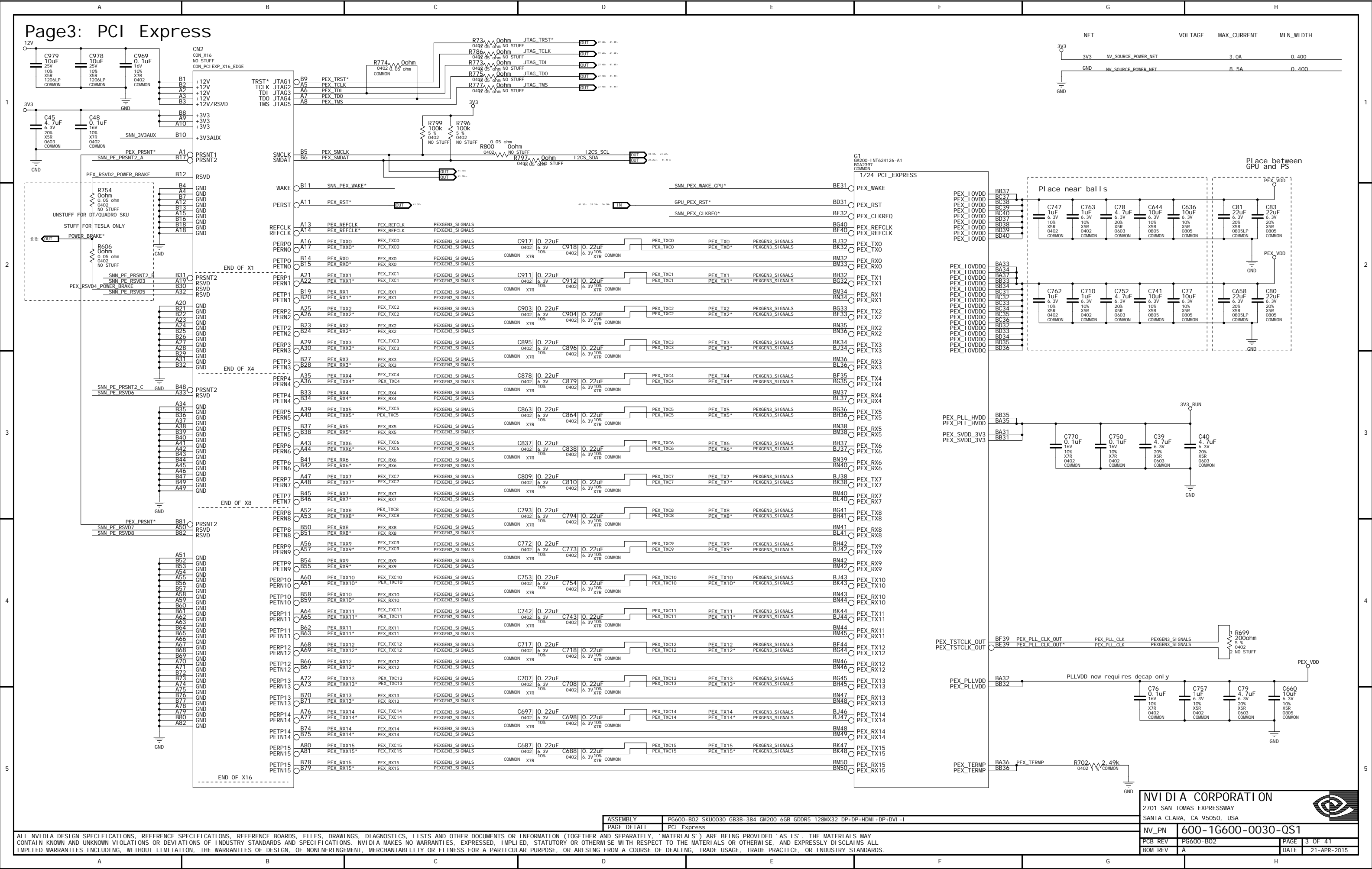
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Page3: PCI Express

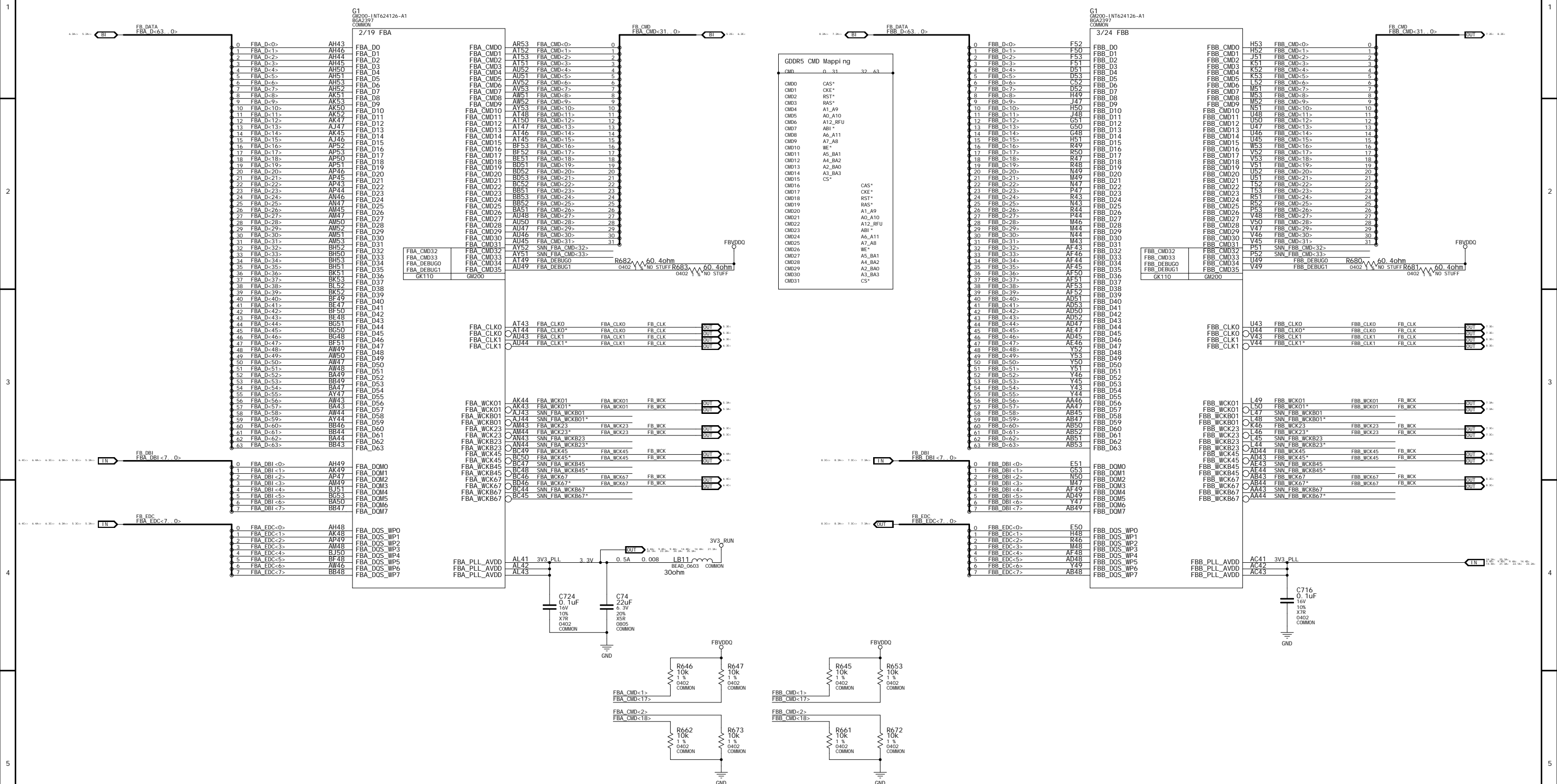


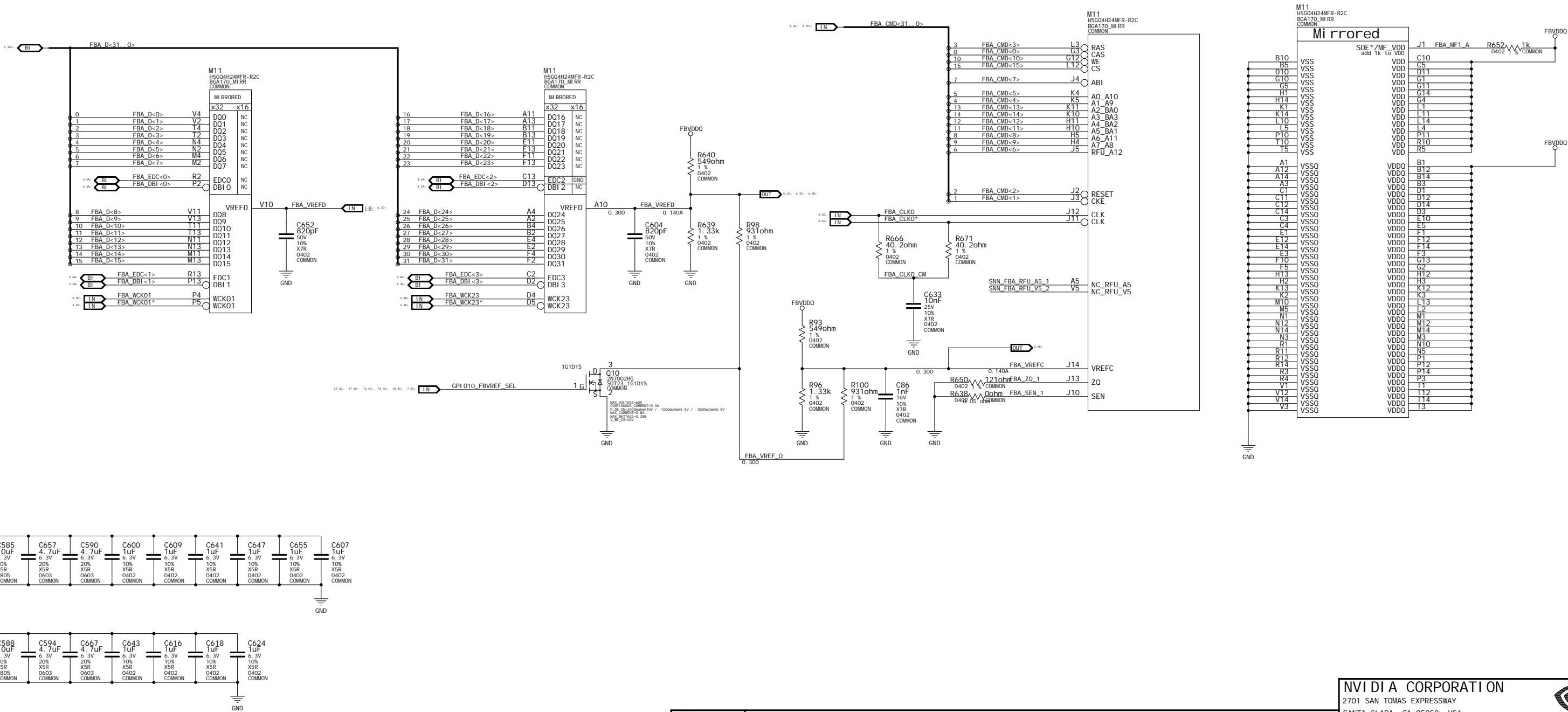
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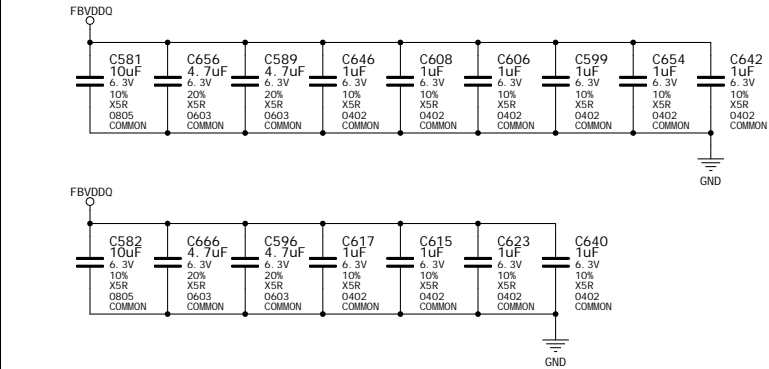
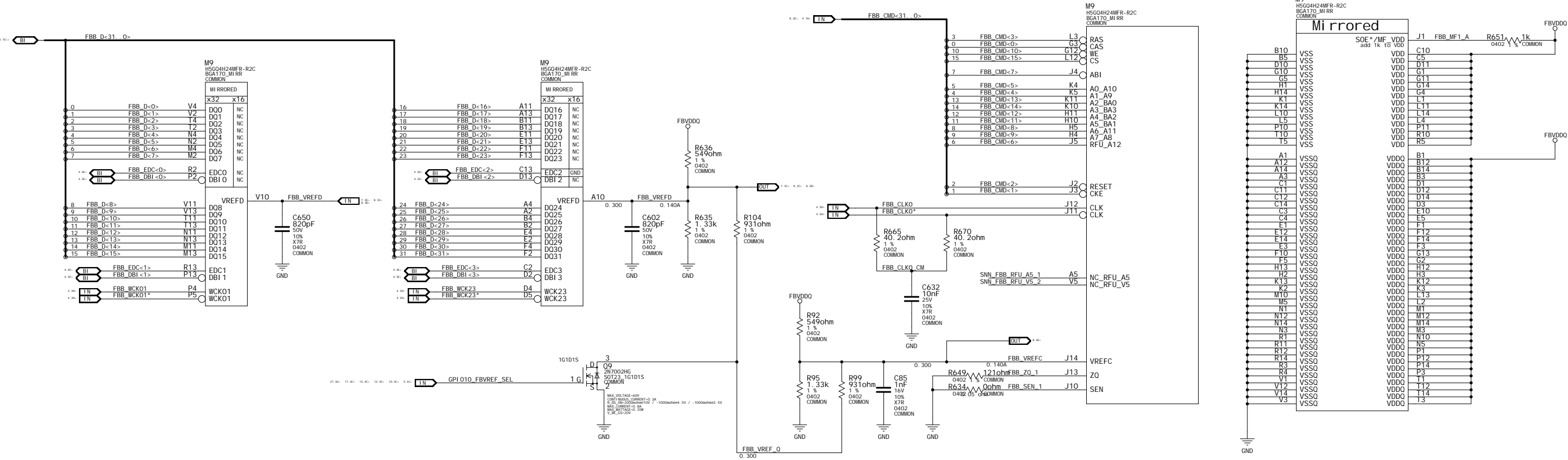
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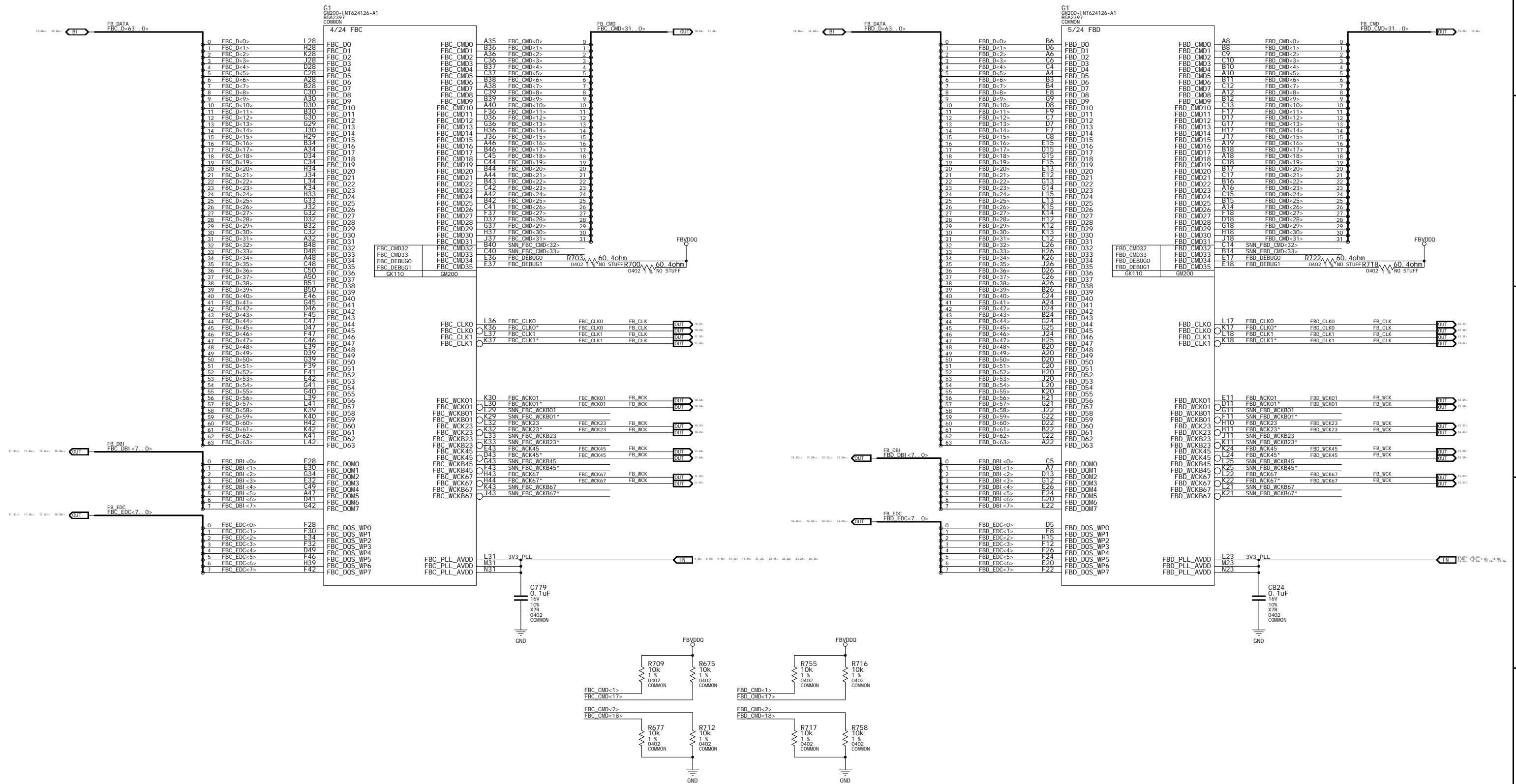


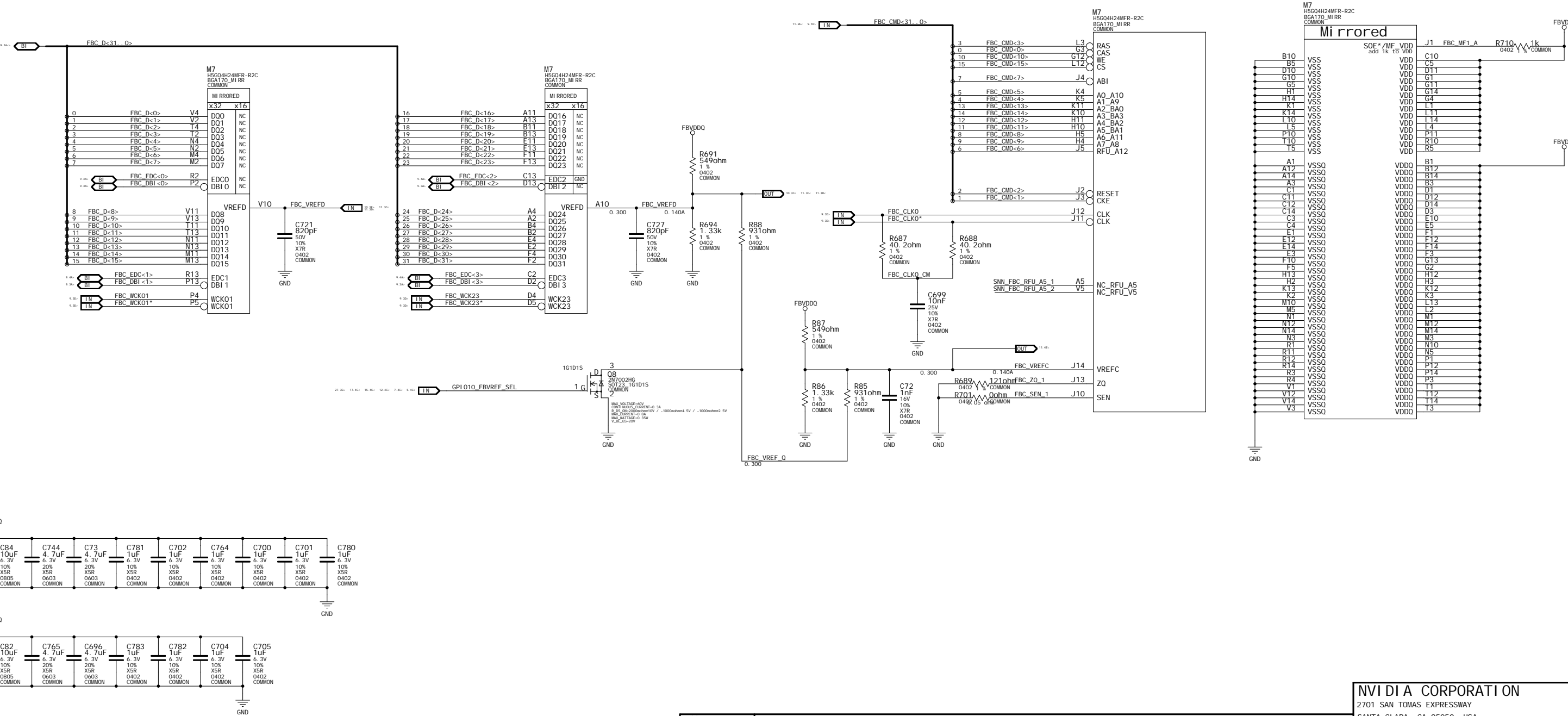


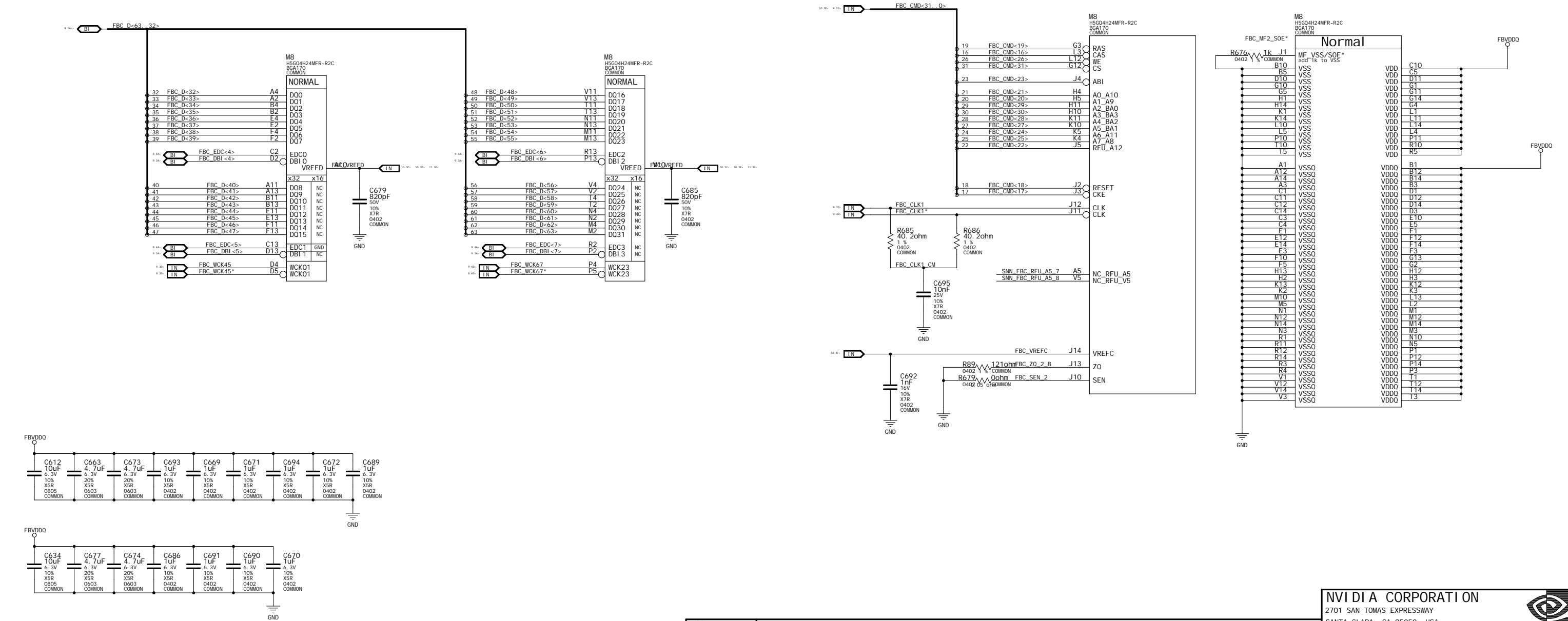
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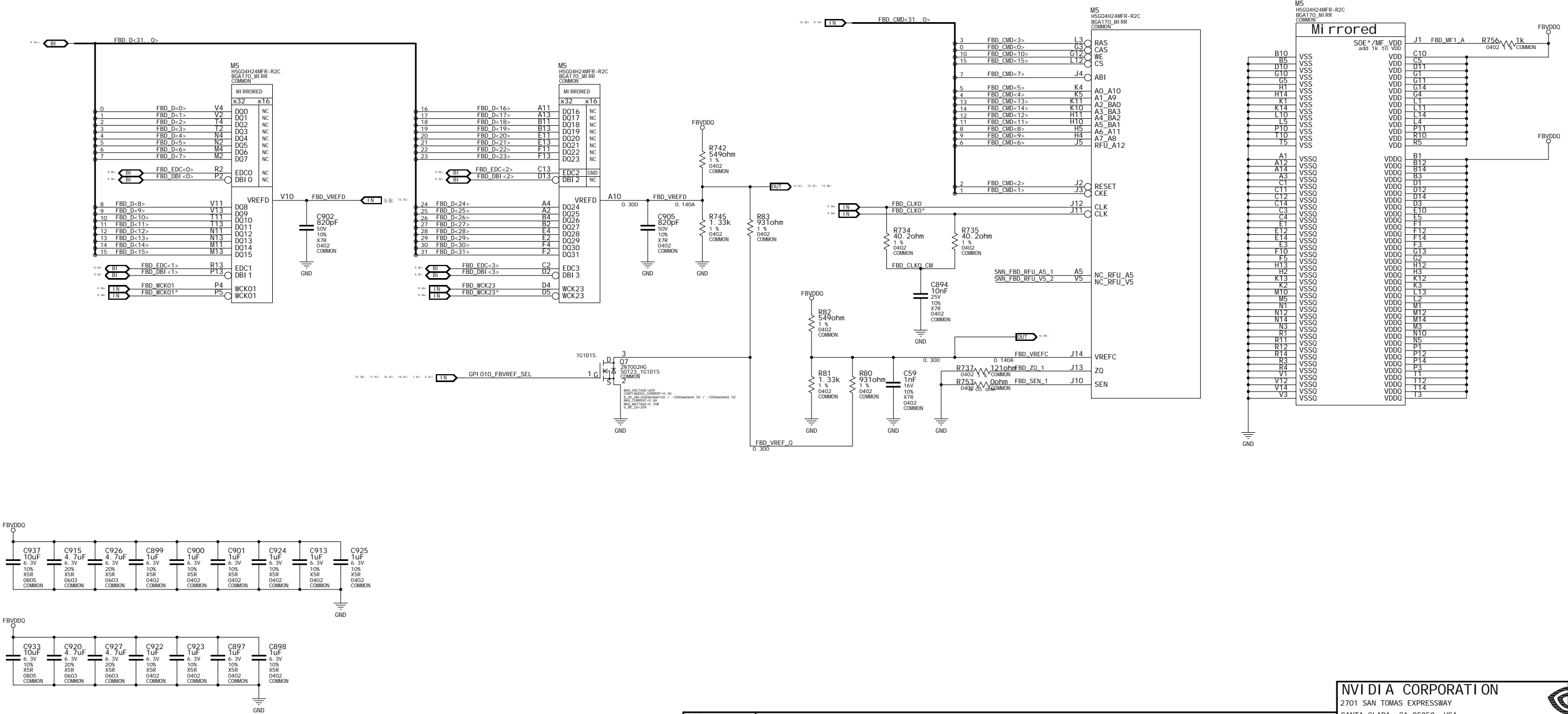


Page9: MEMORY: GPU Partit ion C/D









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ASSEMBLY

PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DV1-1

PAGE DETAIL

MEMORY: FBD[31:0]

NV_PN

600-1G600-0030-QS1

PCB REV

PG600-B02

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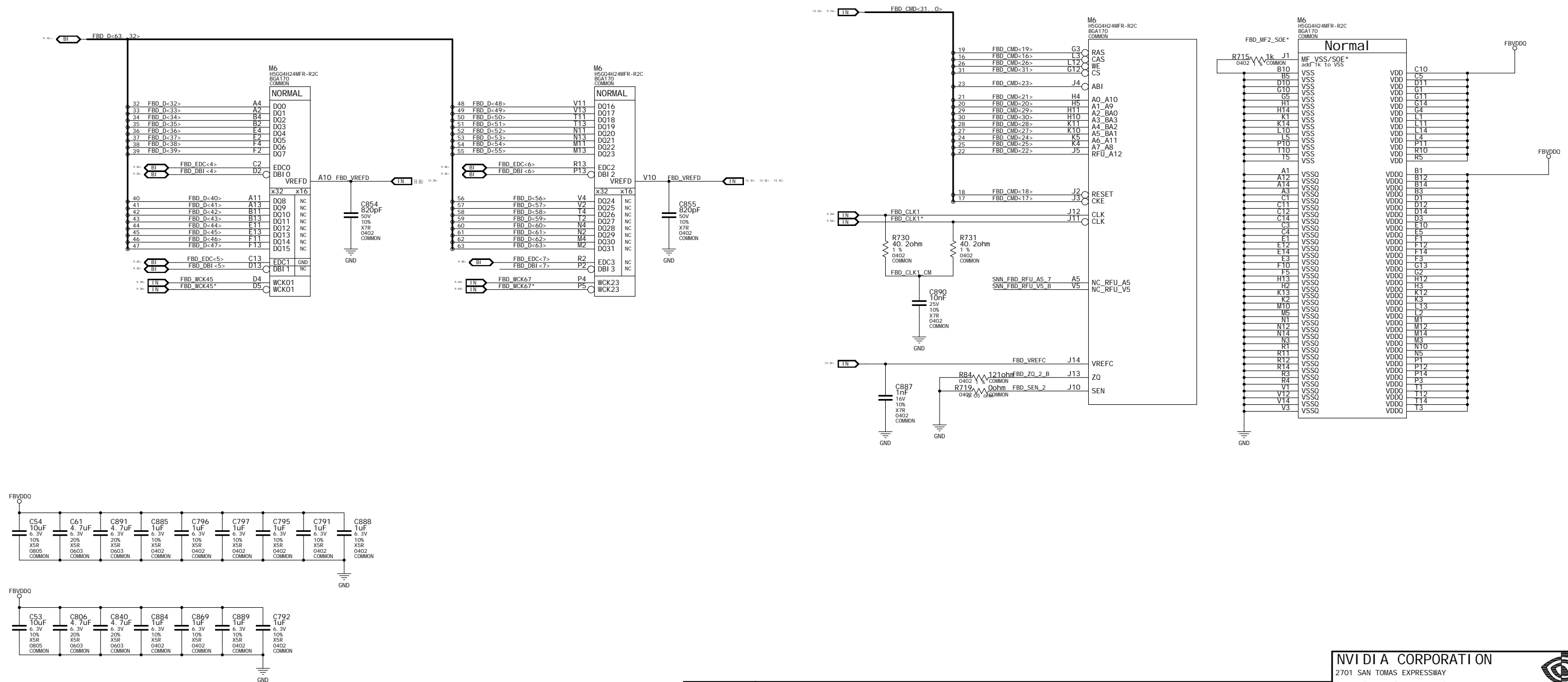
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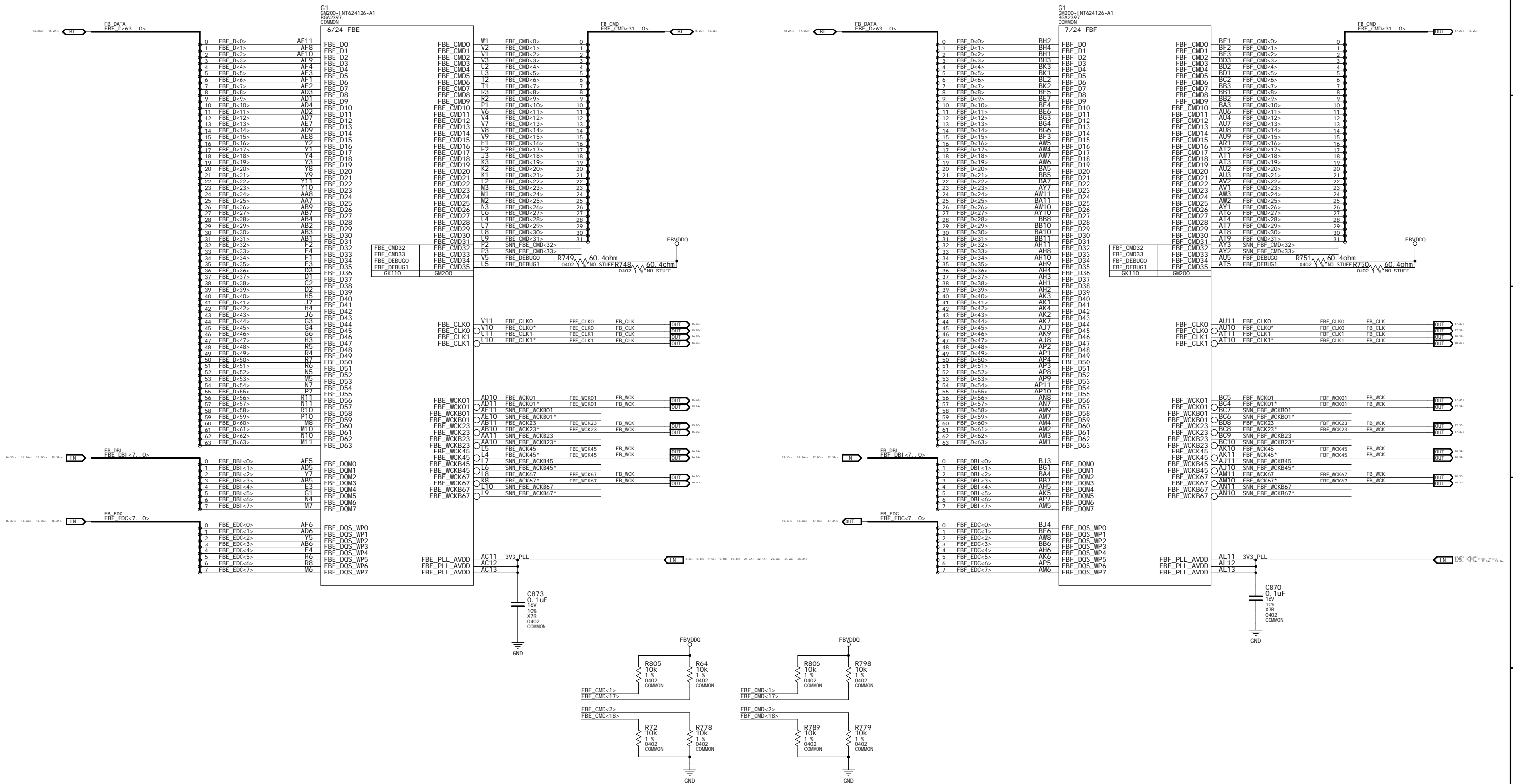
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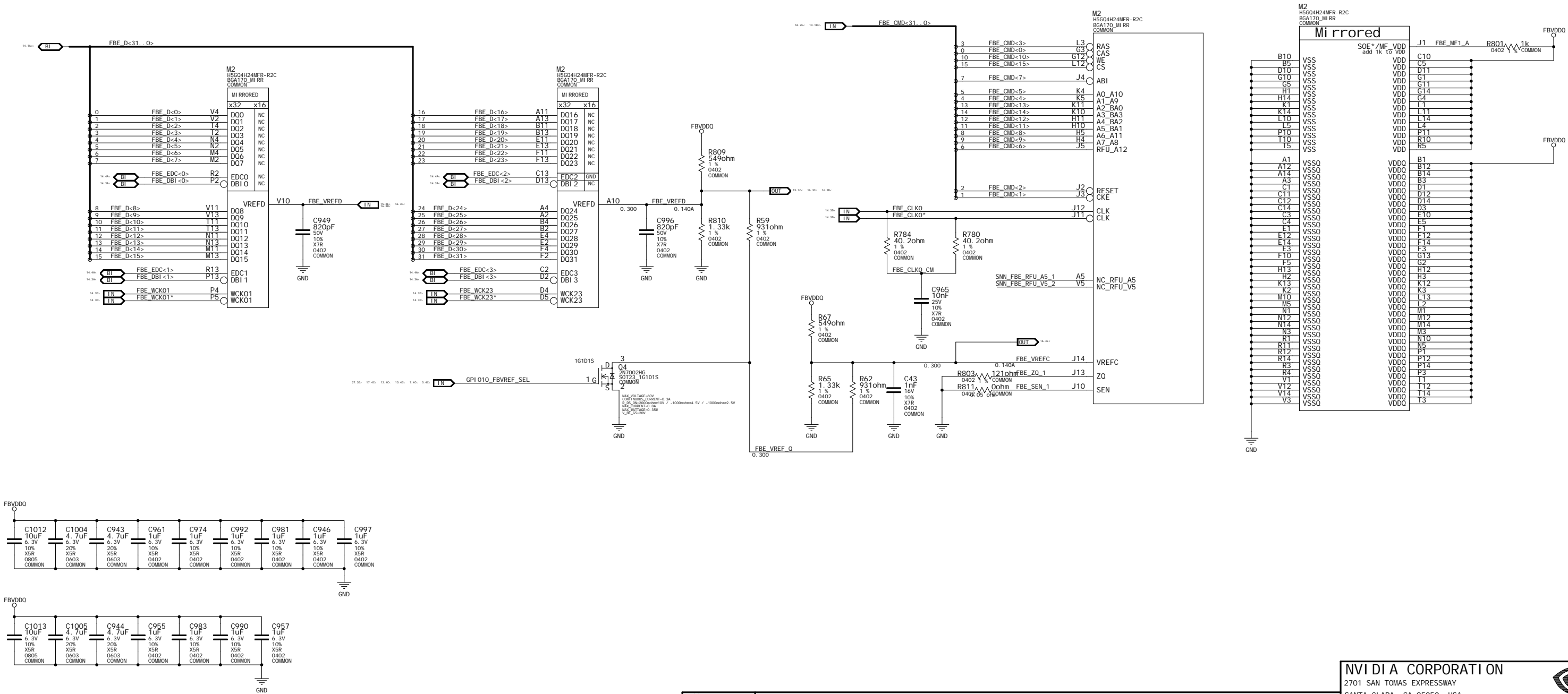
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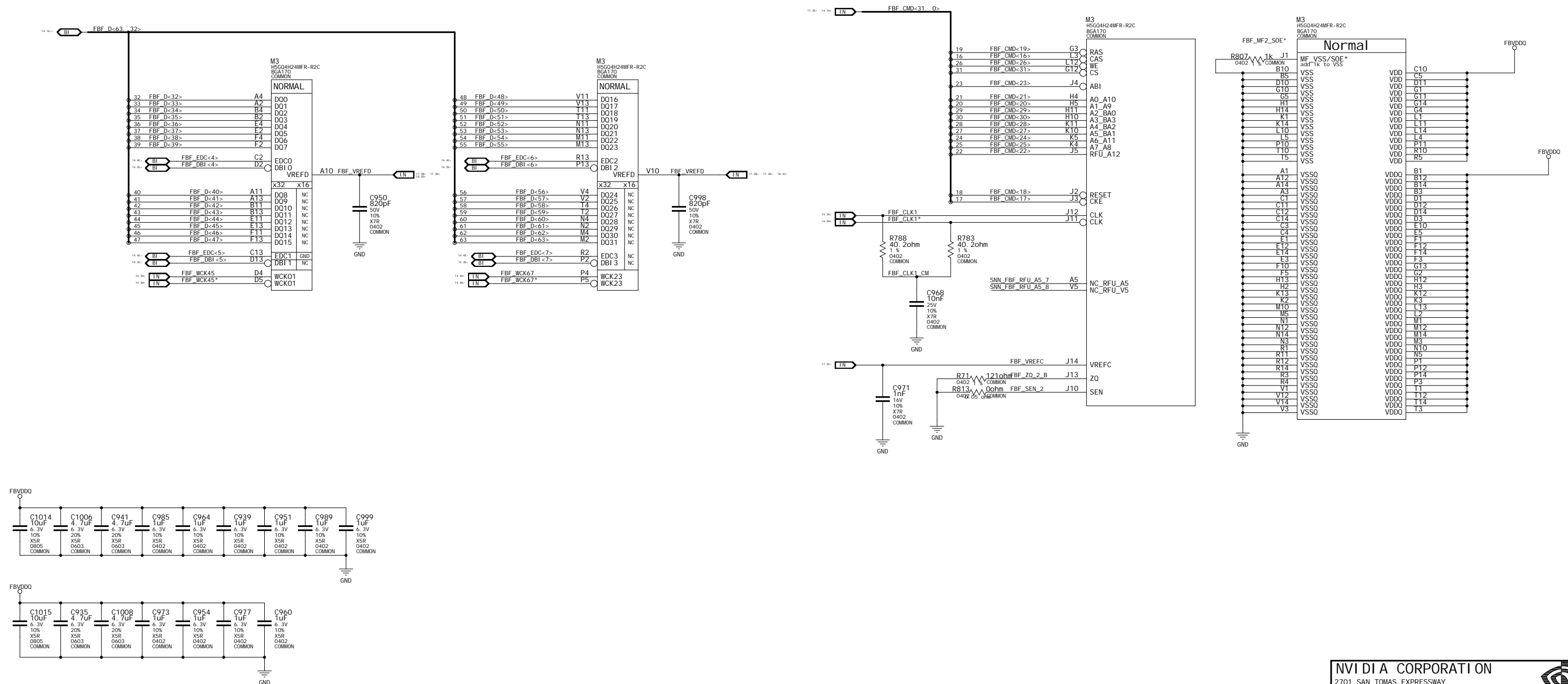




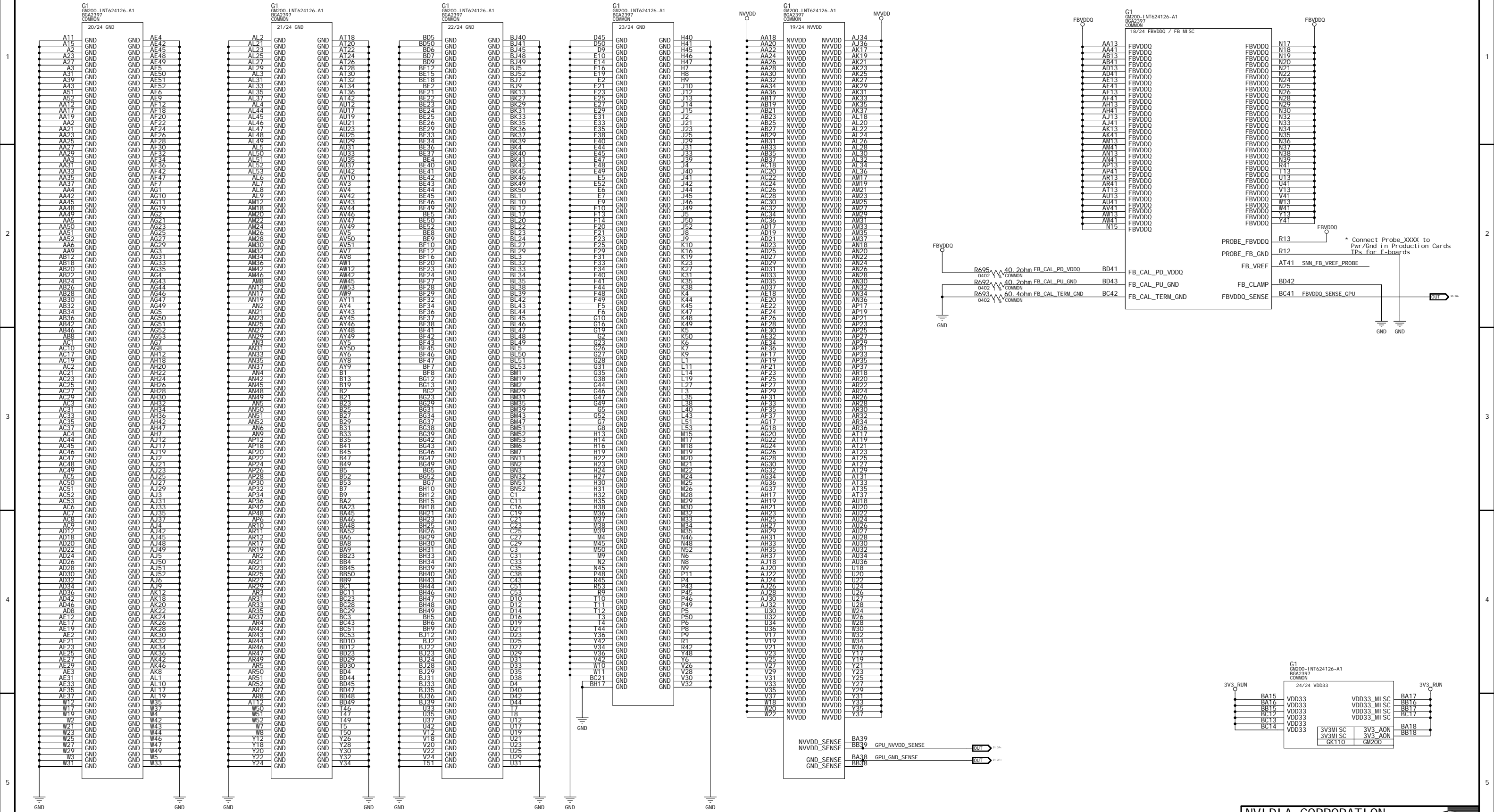


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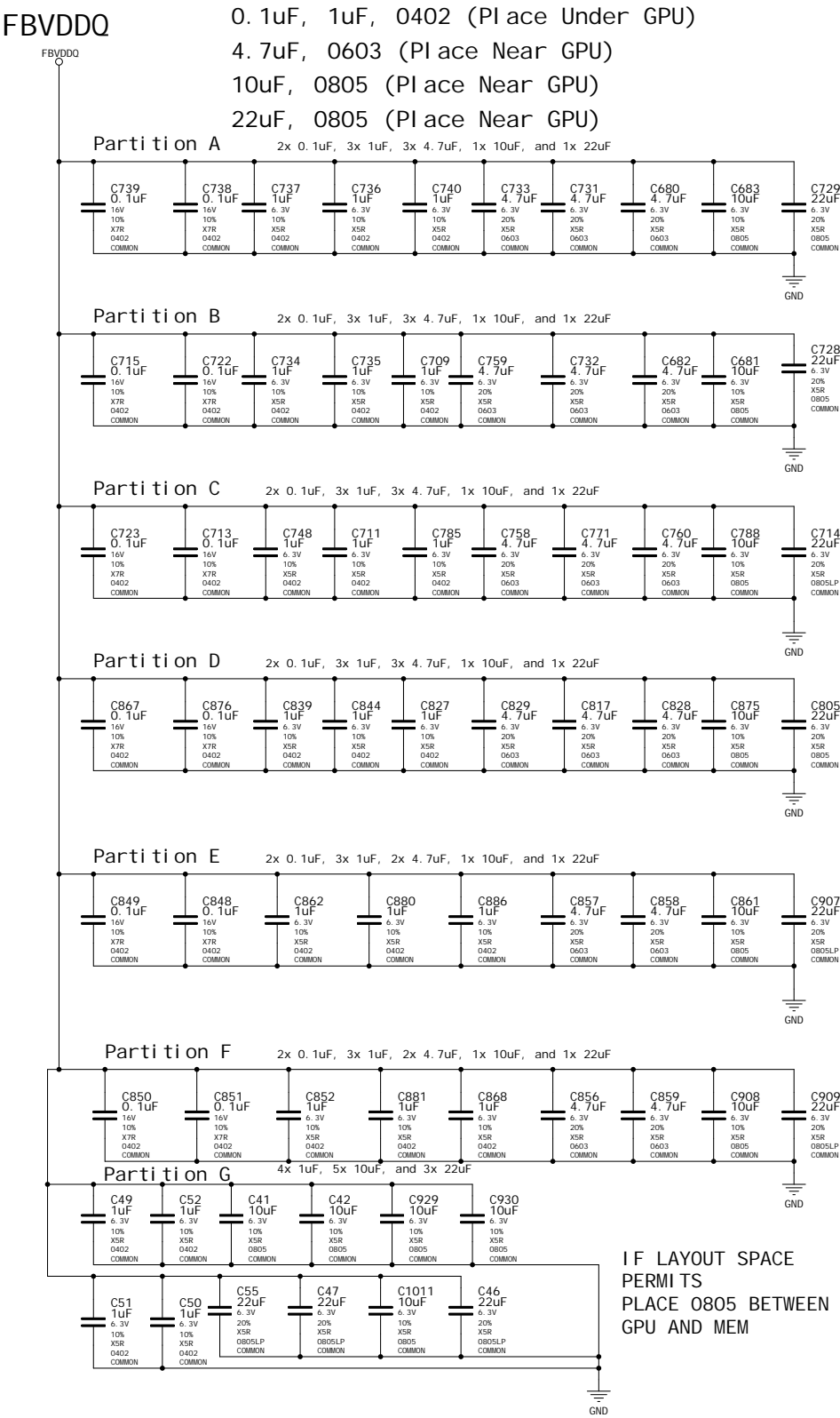




Page19: GPU PWR and GND

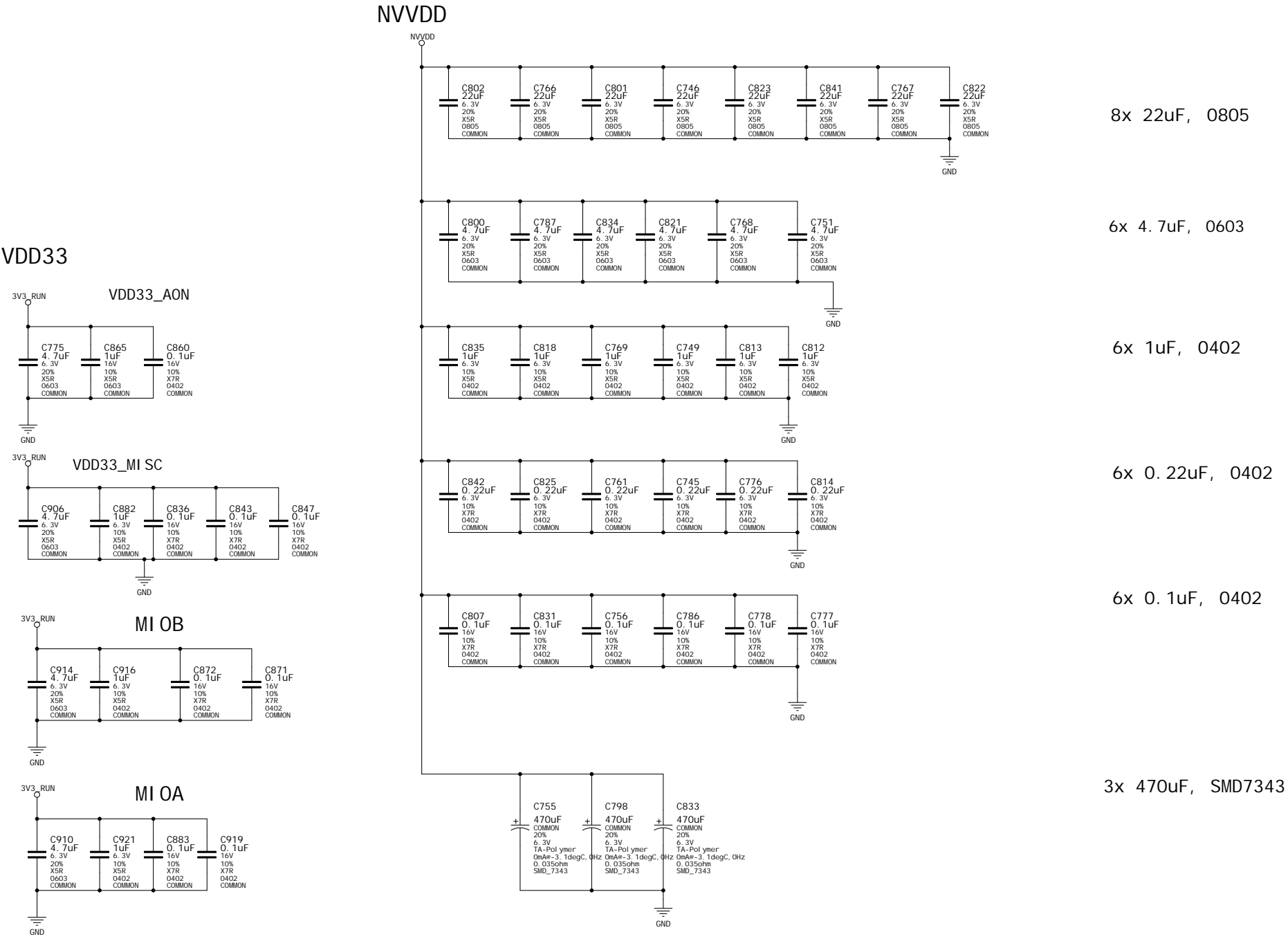


Based on GB3-X GDDR5 FBVDDQ Decap Guideline

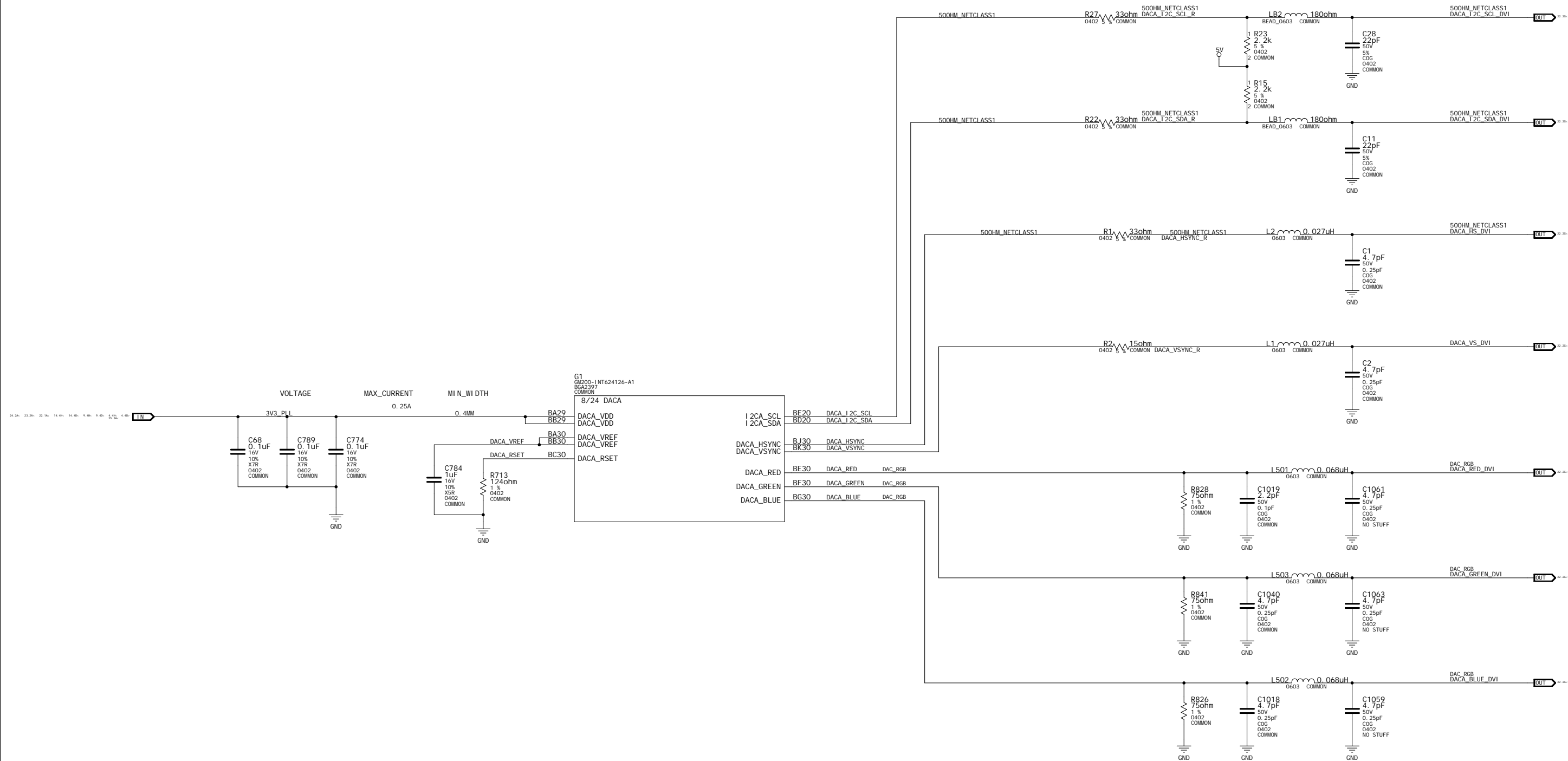


NVVDD Decoupling caps. Place under GPU.

NVVDD



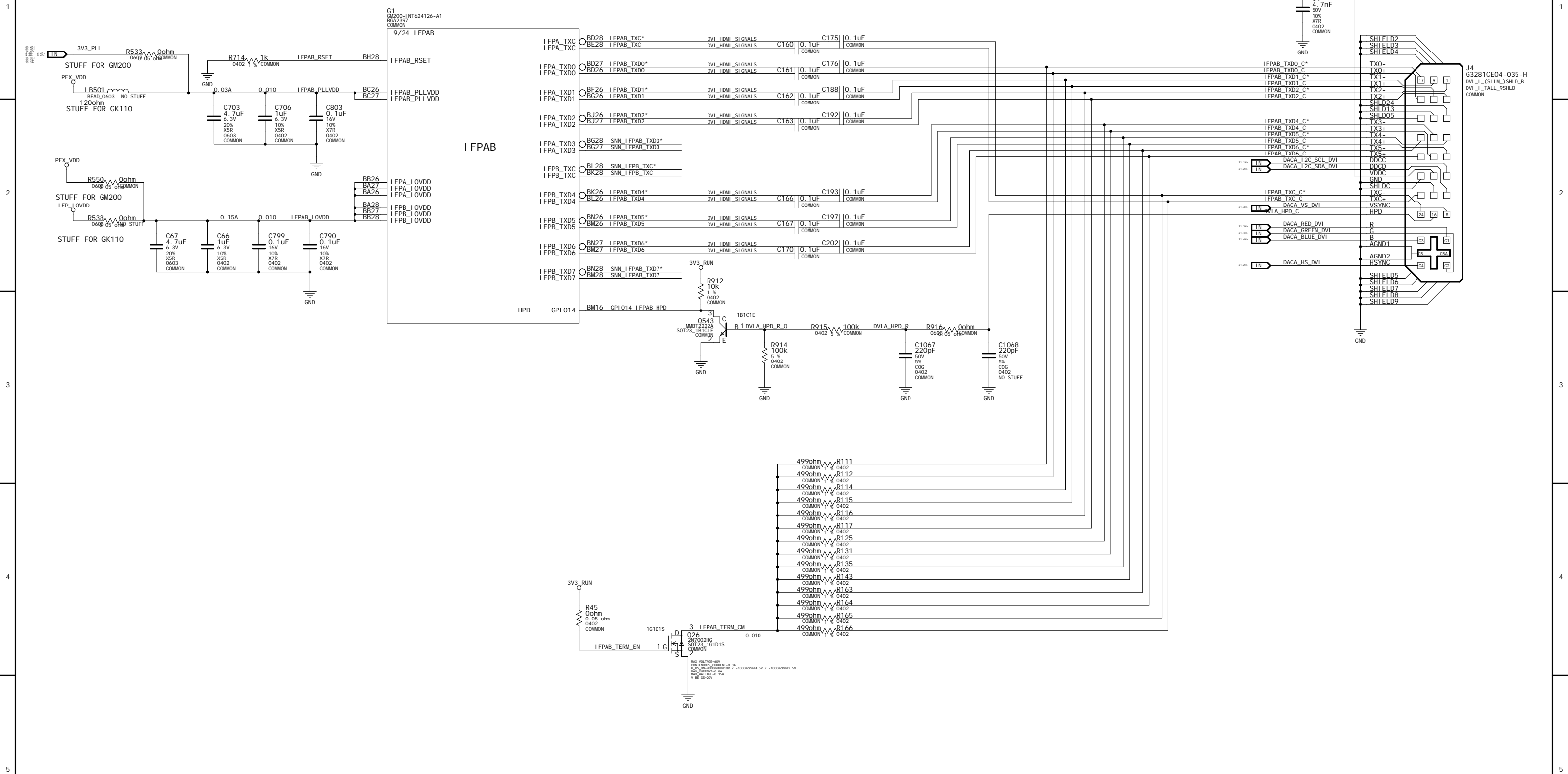
Page21: DACA Interface



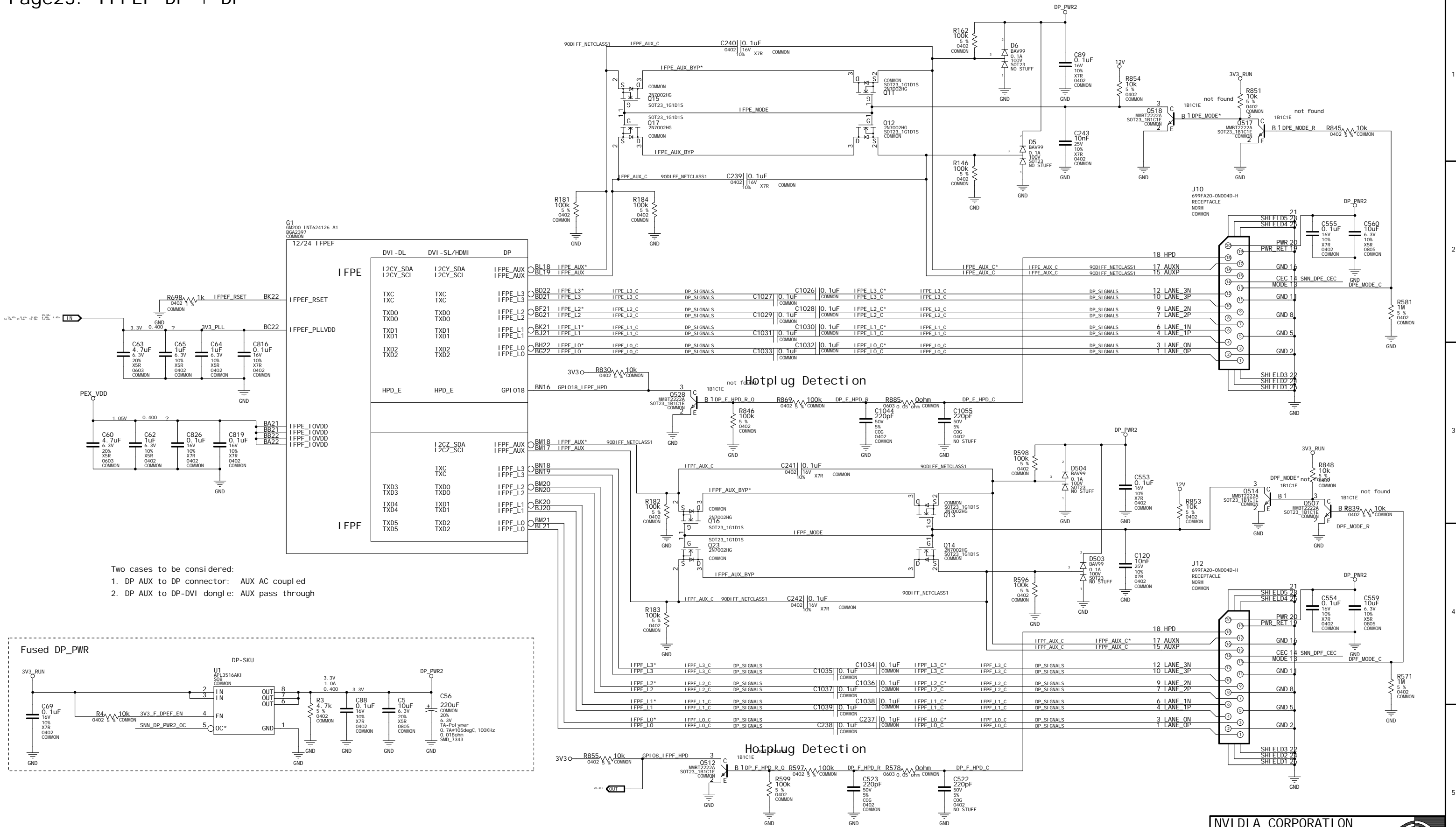
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AC COUPLING NOT NEEDED for KEPLER
REPLACE WITH ZERO OHM RESISTORS FOR KEPLER SKUs



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PAGE DETAIL	1FPEF DP + DP

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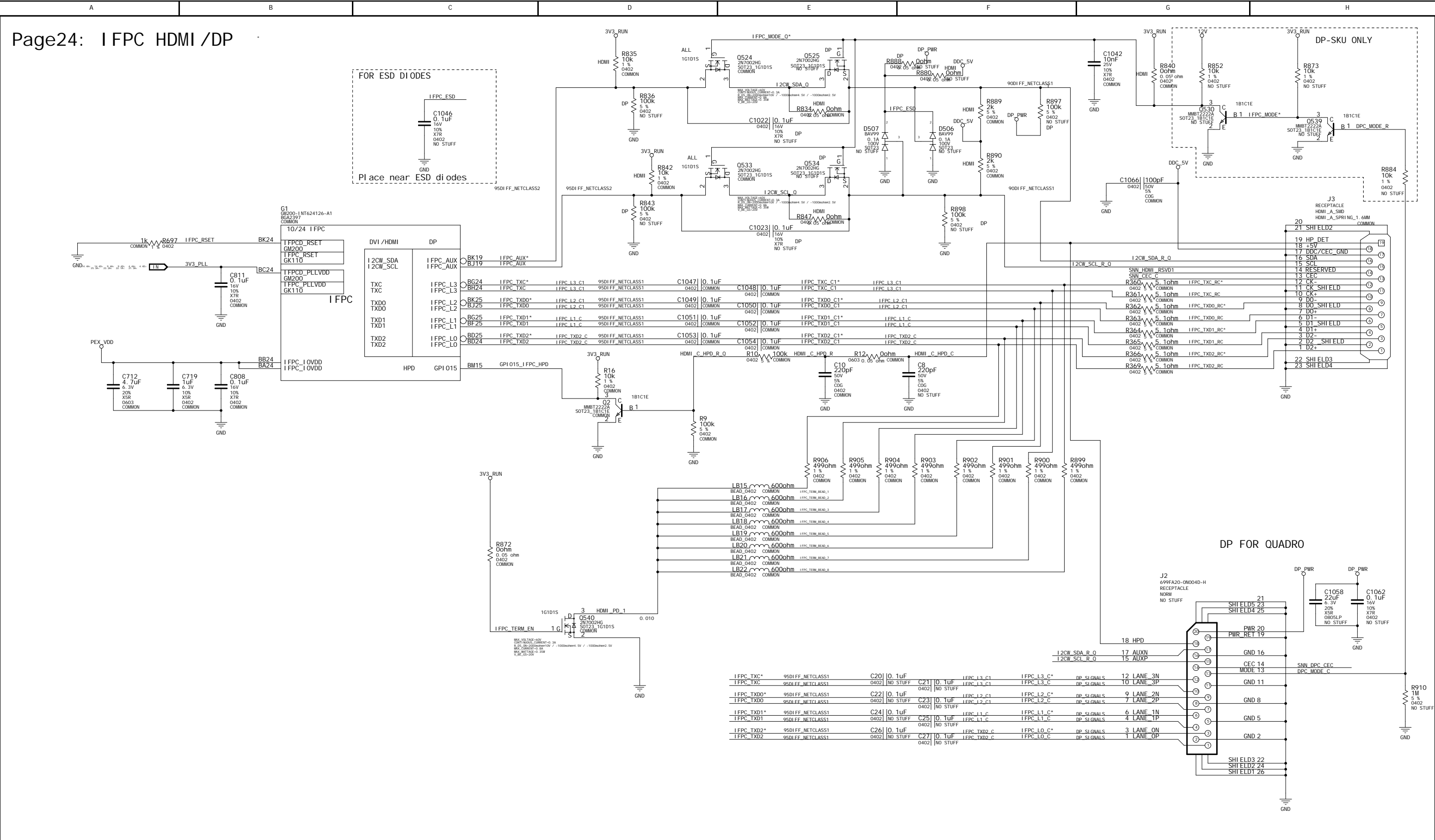
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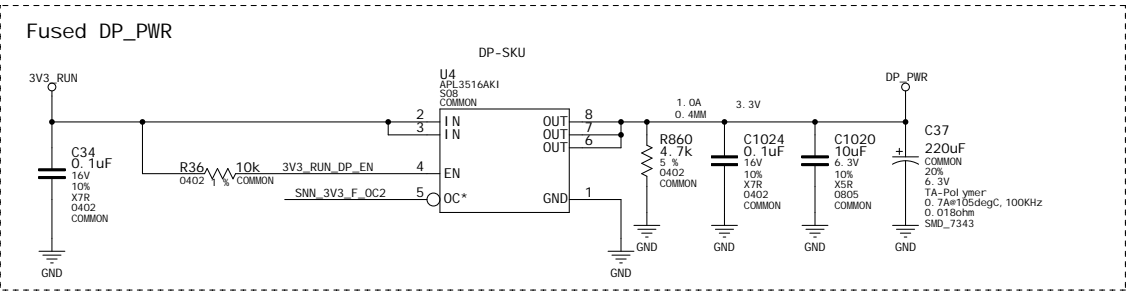
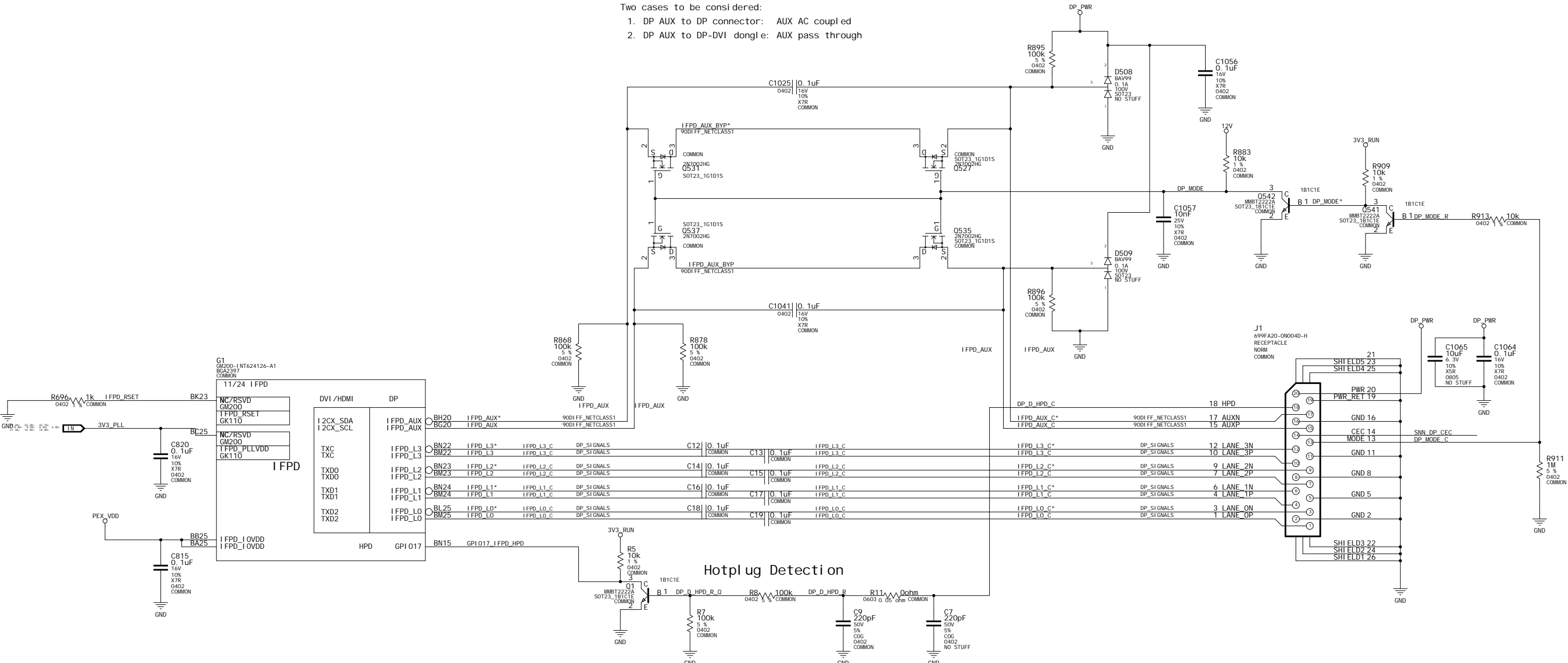
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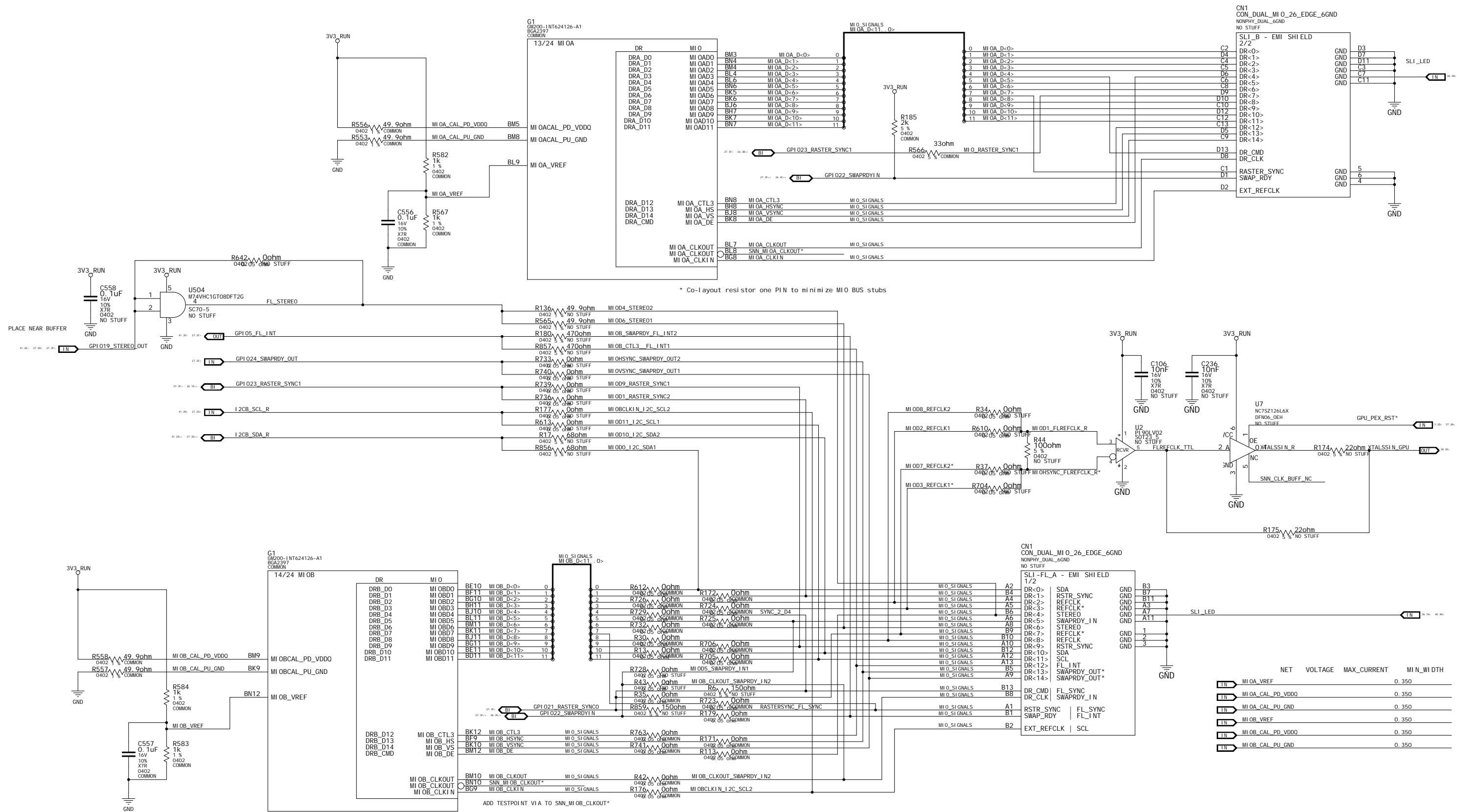
- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through




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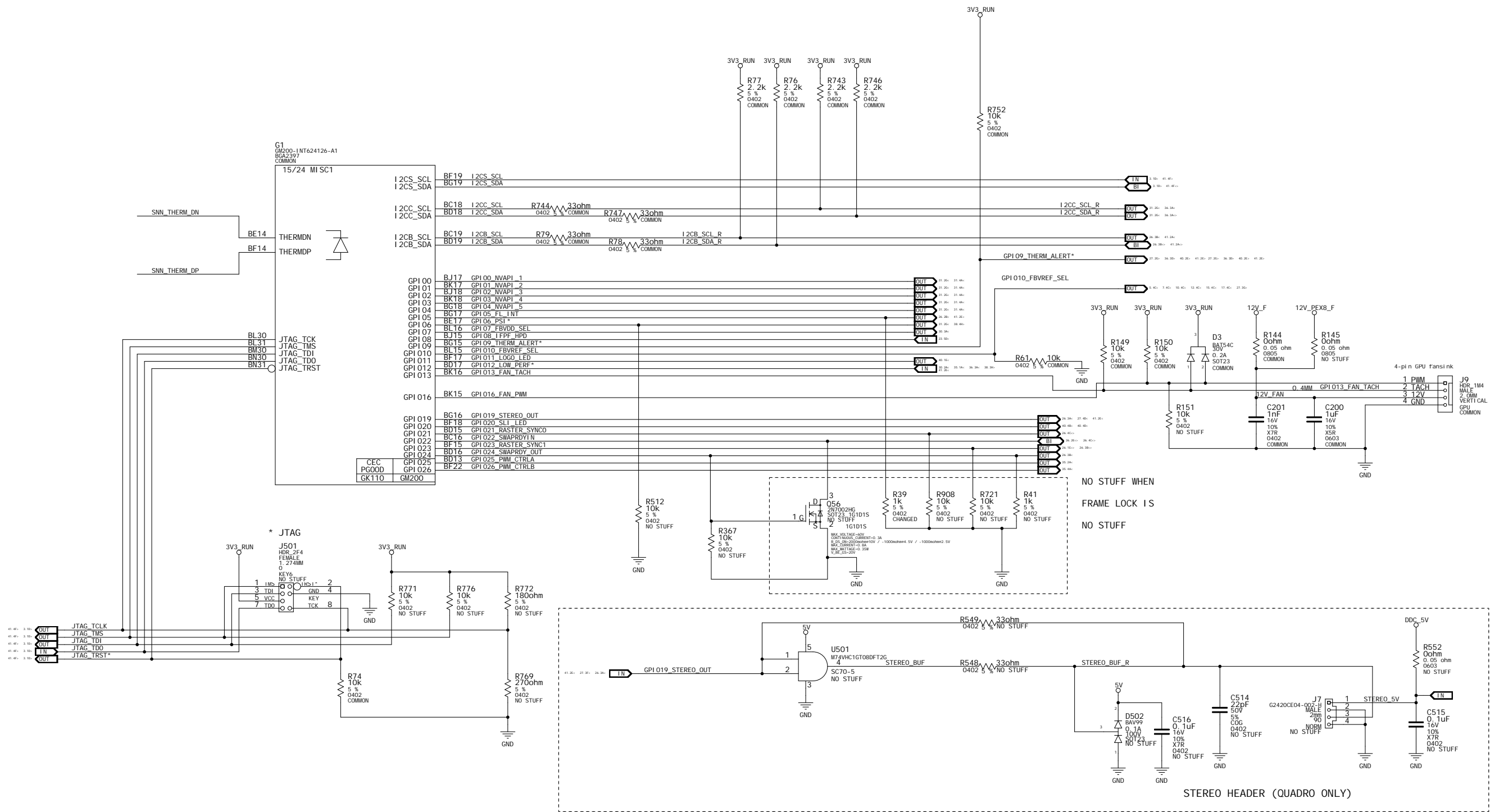
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Page26: MI 0A/B and FRAMELOCK Interface



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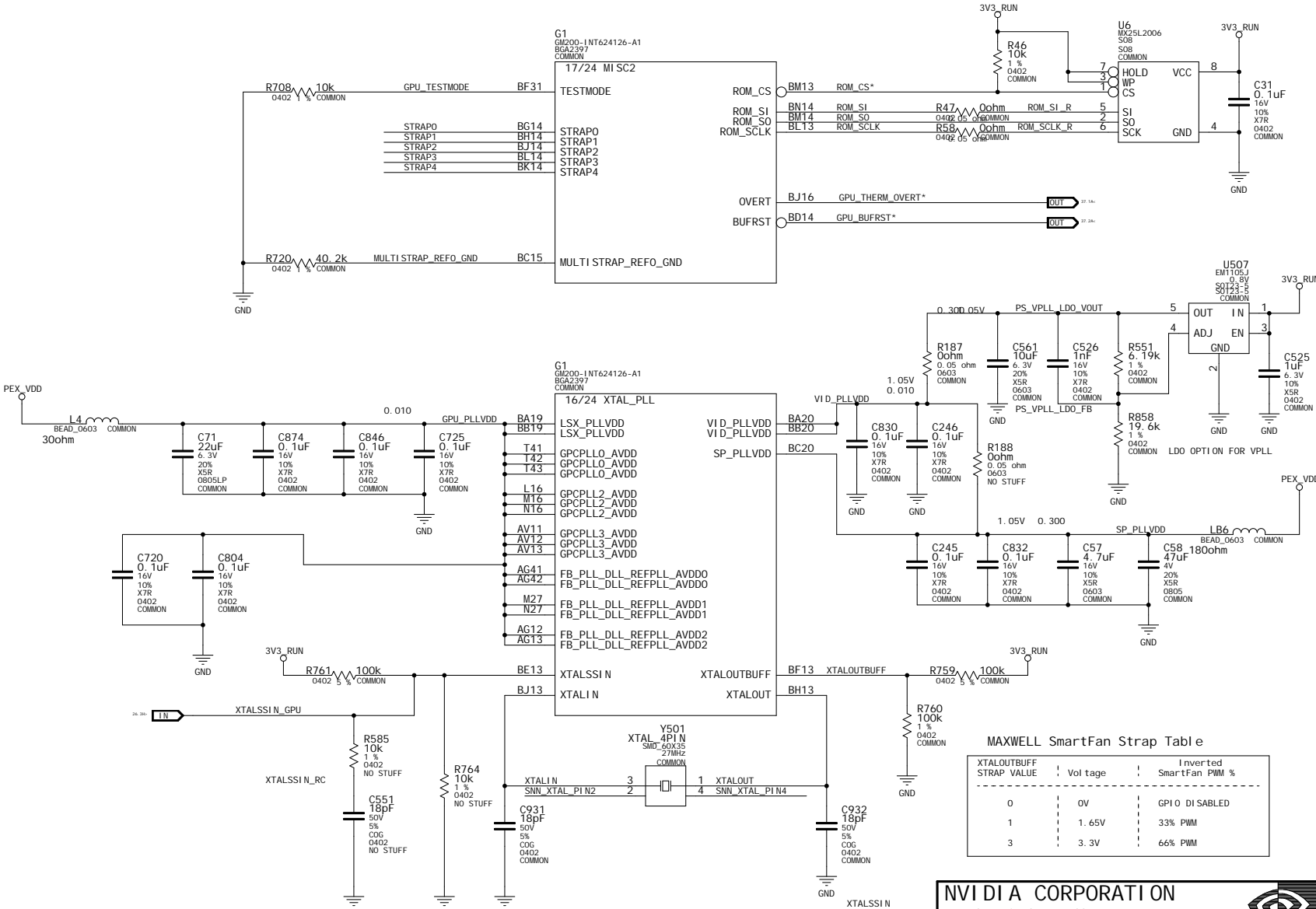
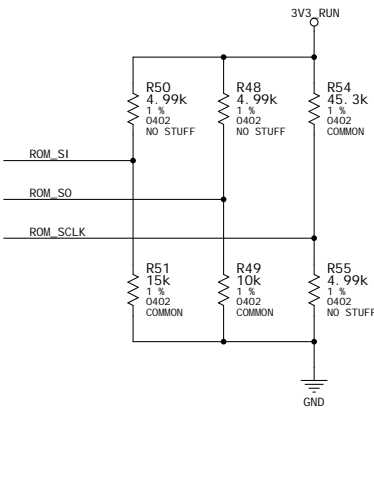
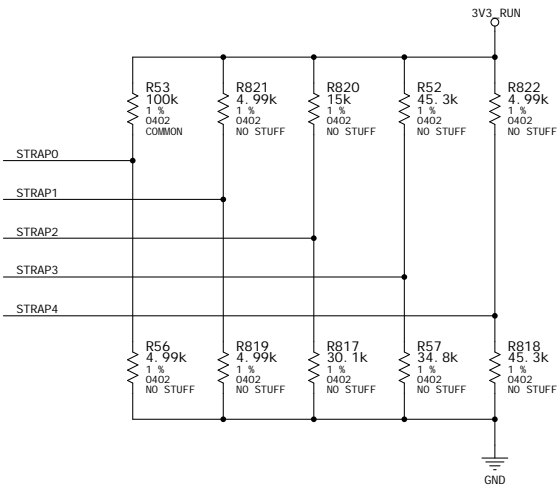


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Page28: MI SC2: ROM, XTAL, Straps

		GK110	GM200
STRAP0	USER_BIT [3:0]*	0000*	GC6_ENABLE(3.3V) PU
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	N/A
STRAP2	PCI_DEVICE [3:0]*	100A*	N/A
STRAP3	SOR_EXPOSED [3:0]*	1111*	N/A
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	N/A
	PEX_MAX_SPEED*	1* FOR GEN2/3*	N/A
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	N/A
	RESERVED	0*	N/A
ROM_SI	RAMCFG[0]*	1*	RAMCFG[0]*
	RAMCFG[1]*	0*	RAMCFG[1]*
	RAMCFG[2]*	1*	RAMCFG[2]*
	RAMCFG[3]*	0*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	1*	VGA_DEVICE* 1* For Enable
	SMB_ALT_ADDR*	0*	SMB_ALT_ADDR 0* For Disable
	FB[0]_APERTURE_SIZE*	1* For 128MB*	PCI_CFG 0* For Desktop
	FB[1]_APERTURE_SIZE*	0* For 128MB*	DEVICE_SEL 0* For DEVICE A
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLED*	SOR0_EXPOSED
	PCI_DEVICE_EXT[5]*	0*	SOR1_EXPOSED
	SUB_VENDOR*	1* Dedicated BIOS*	SOR2_EXPOSED
	PCI_DEVICE_EXT[4]*	0*	SOR3_EXPOSED

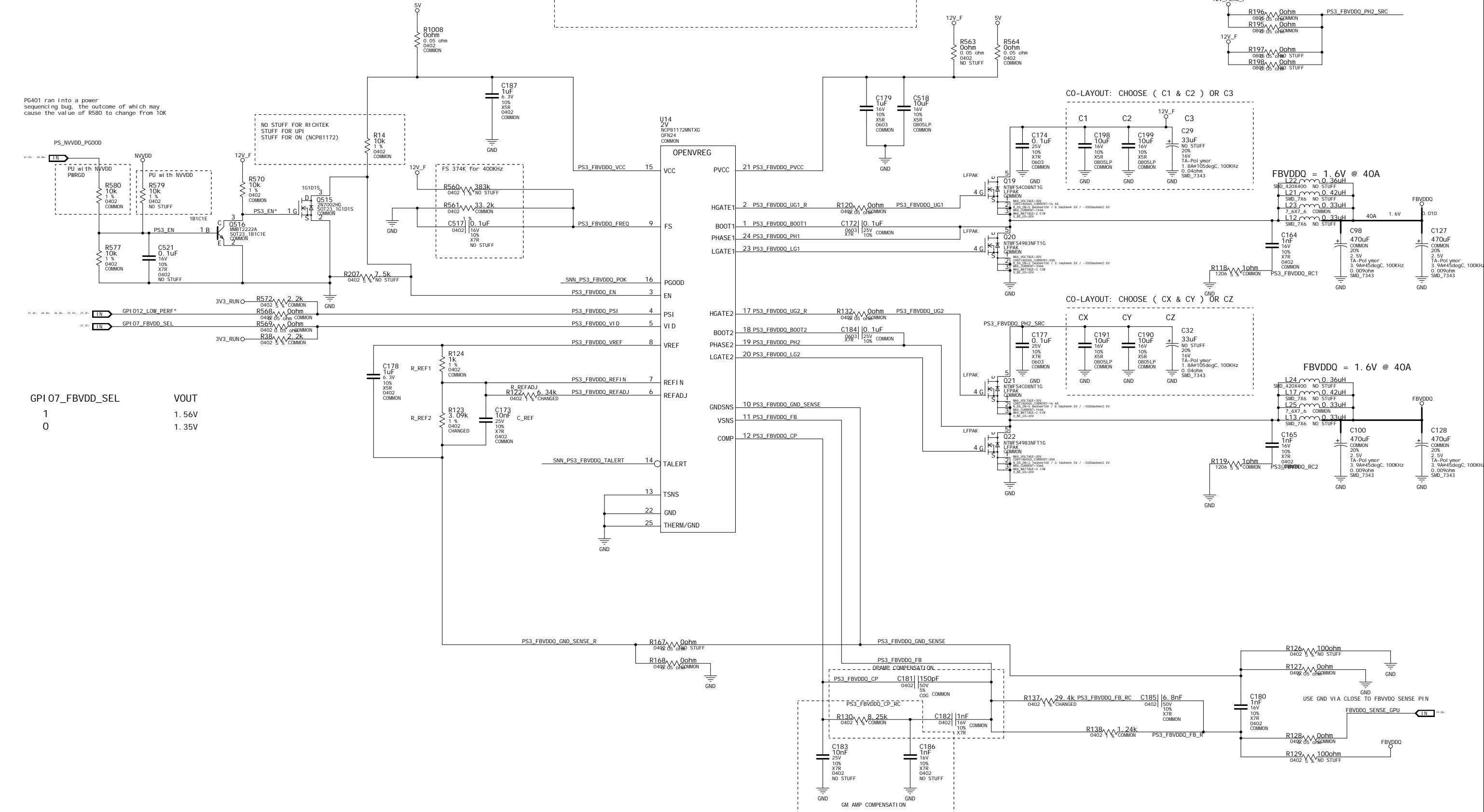
BINARY PRODUCTION	MULTI_STRAP_REFO_GND
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND



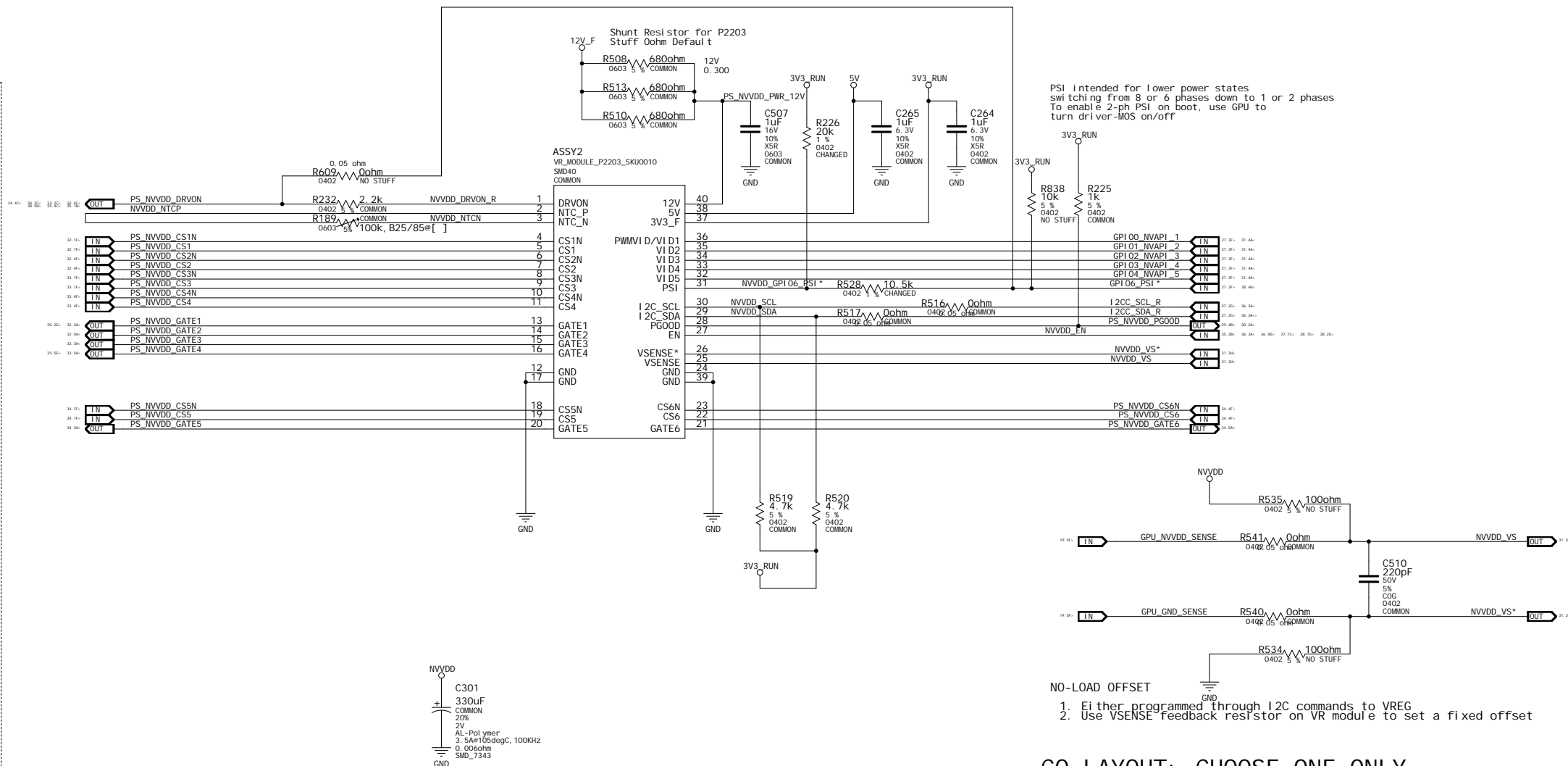
MAXWELL SmartFan Strap Table		
XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	1.65V	33% PWM
3	3.3V	66% PWM

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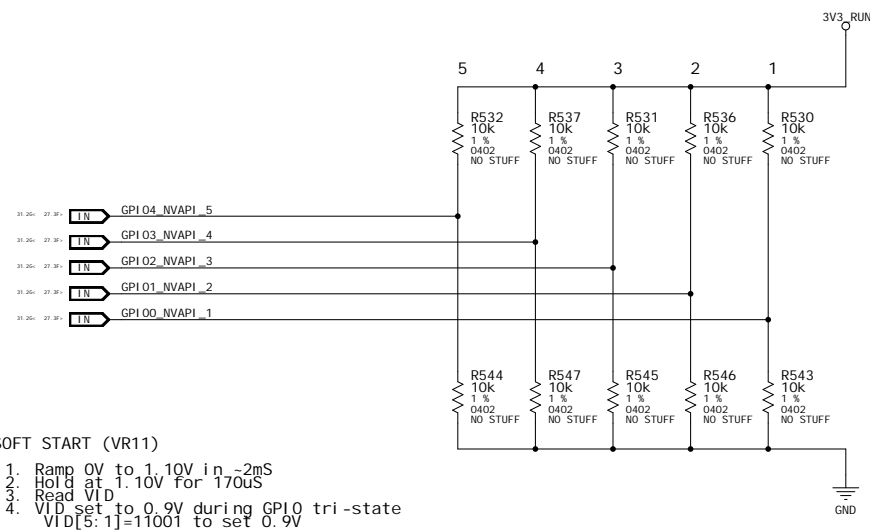


V I D Table					
GPI 04	GPI 03	GPI 02	GPI 01	GPI 00	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1. 2125V
0	0	0	0	1	1. 2000V
0	0	0	1	0	1. 1875V
0	0	0	1	1	1. 1750V
0	0	1	0	0	1. 1625V
0	0	1	0	1	1. 1500V
0	0	1	1	0	1. 1375V
0	0	1	1	1	1. 1250V
0	1	0	0	0	1. 1125V
0	1	0	0	1	1. 1000V
0	1	0	1	0	1. 0875V
0	1	0	1	1	1. 0750V
0	1	1	0	0	1. 0625V
0	1	1	0	1	1. 0500V
0	1	1	1	0	1. 0375V
0	1	1	1	1	1. 0250V
1	0	0	0	0	1. 0125V
1	0	0	0	1	1. 0000V
1	0	0	1	0	0. 9875V
1	0	0	1	1	0. 9750V
1	0	1	0	0	0. 9625V
1	0	1	0	1	0. 9500V
1	0	1	1	0	0. 9375V
1	0	1	1	1	0. 9250V
1	1	0	0	0	0. 9125V
1	1	0	0	1	0. 9000V
1	1	0	1	0	0. 8875V
1	1	0	1	1	0. 8750V
1	1	1	0	0	0. 8625V
1	1	1	0	1	0. 8500V
1	1	1	1	0	0. 8375V
1	1	1	1	1	0. 8250V



CO-LAYOUT: CHOOSE ONE ONLY

1. Either programmed through I2C commands to VREG
2. Use VSENSE feedback resistor on VR module to set a fixed offset



SOFT START (VR11)

1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read VID
4. VID set to 0.9V during GPIO tri-state
VID[5:1]=11001 to set 0.9V

P-STATE VOLTAGES

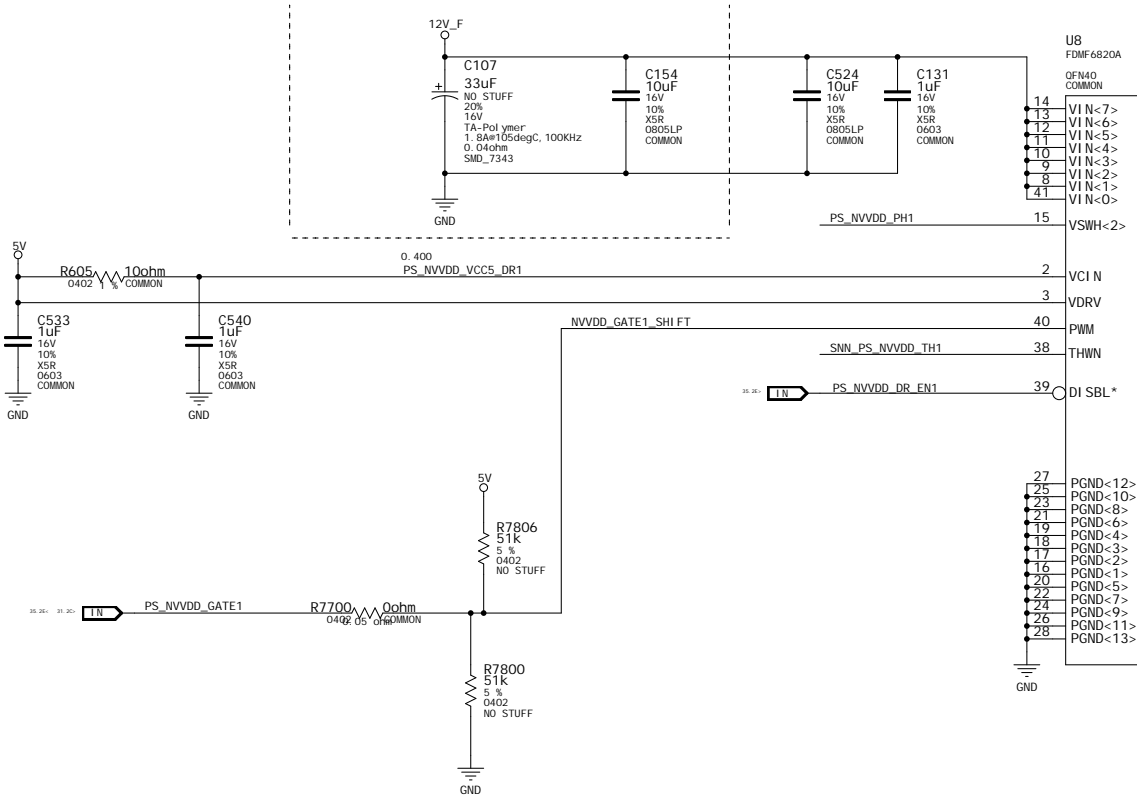
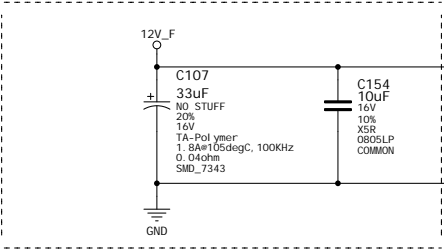
1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI +DP+DVI -
PAGE DETAIL	PS: NVVDD Controller

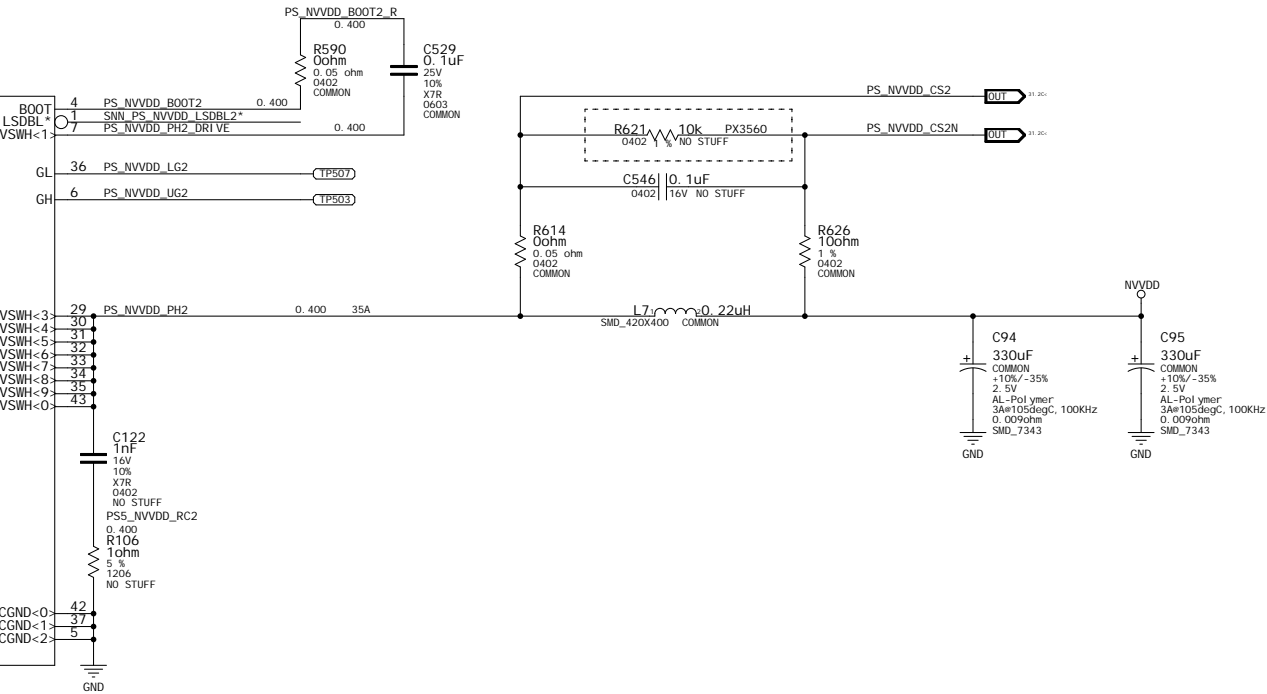
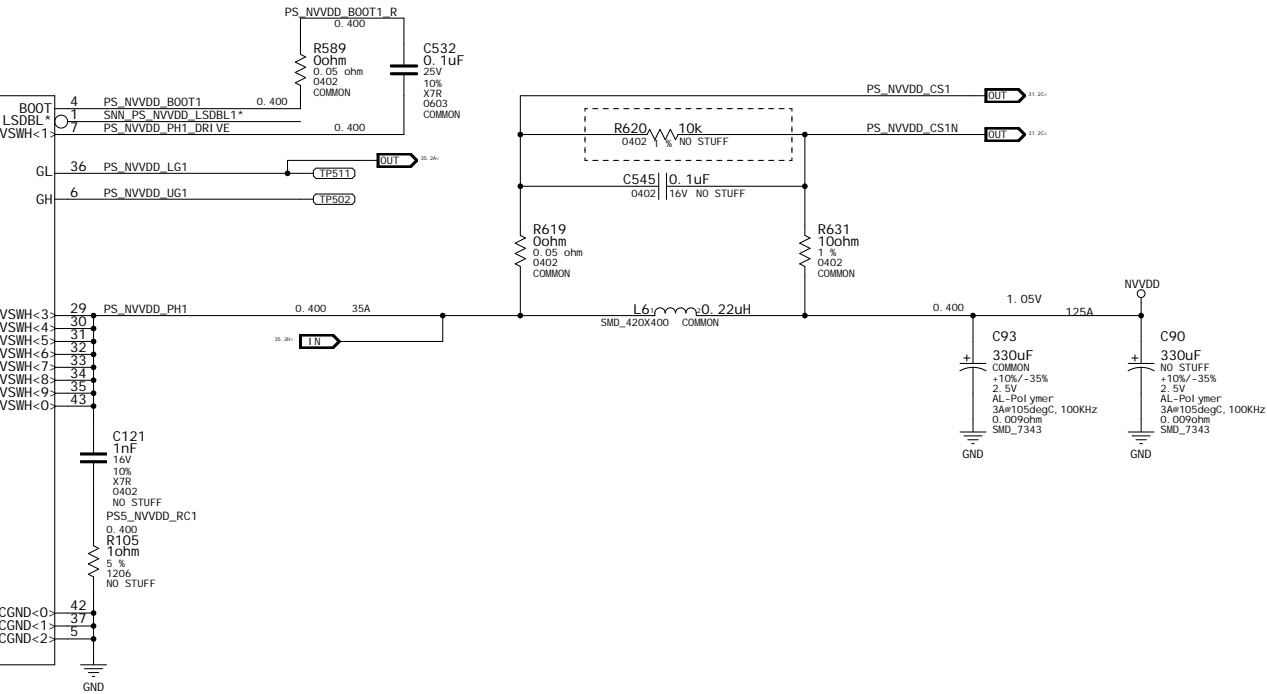
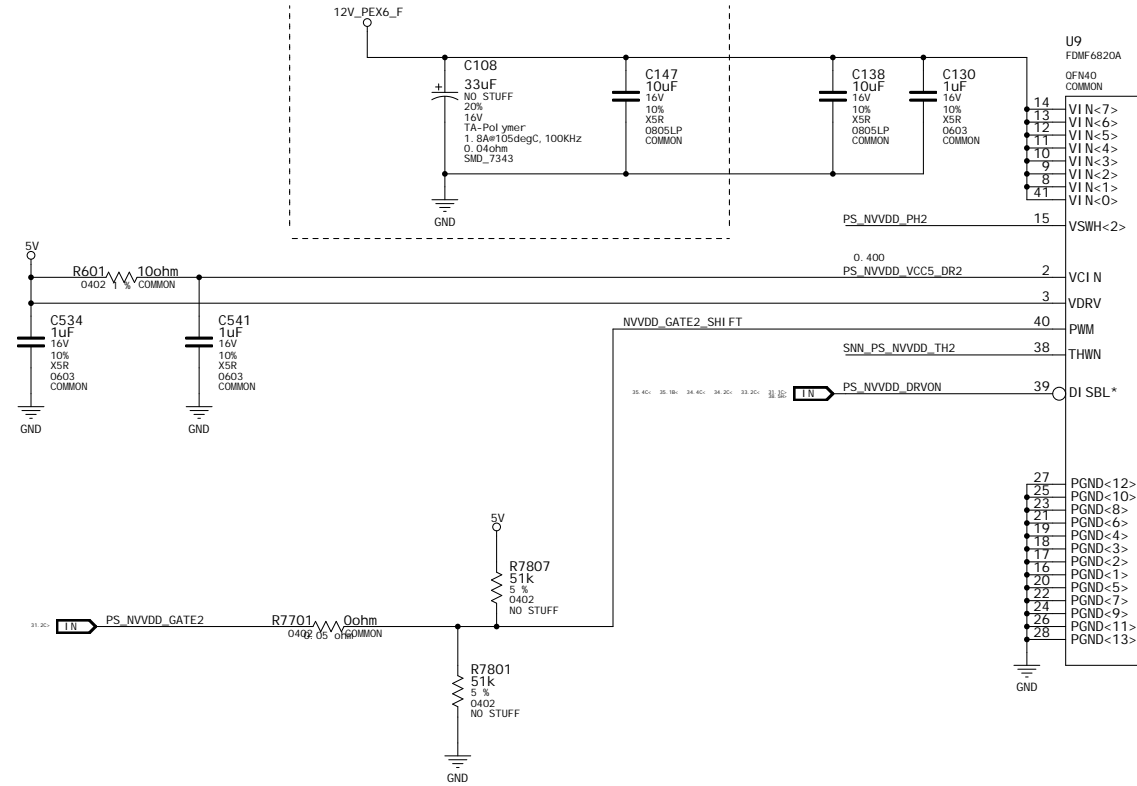
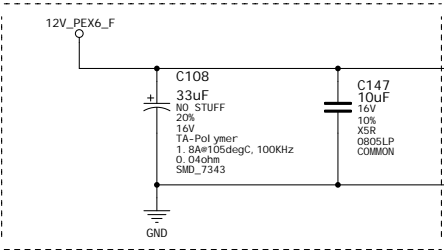
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CO-LAYOUT: STUFF ONLY ONE



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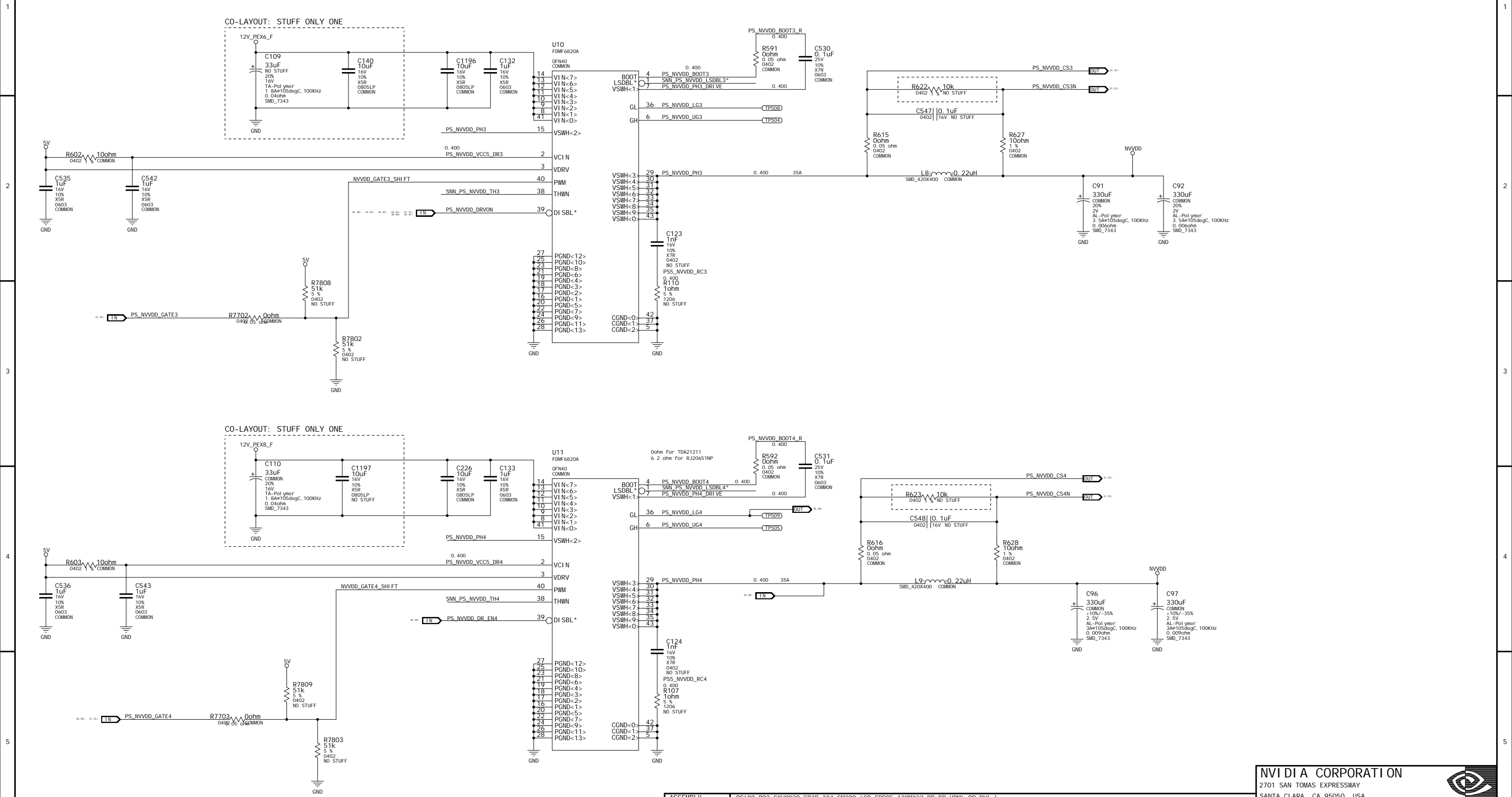
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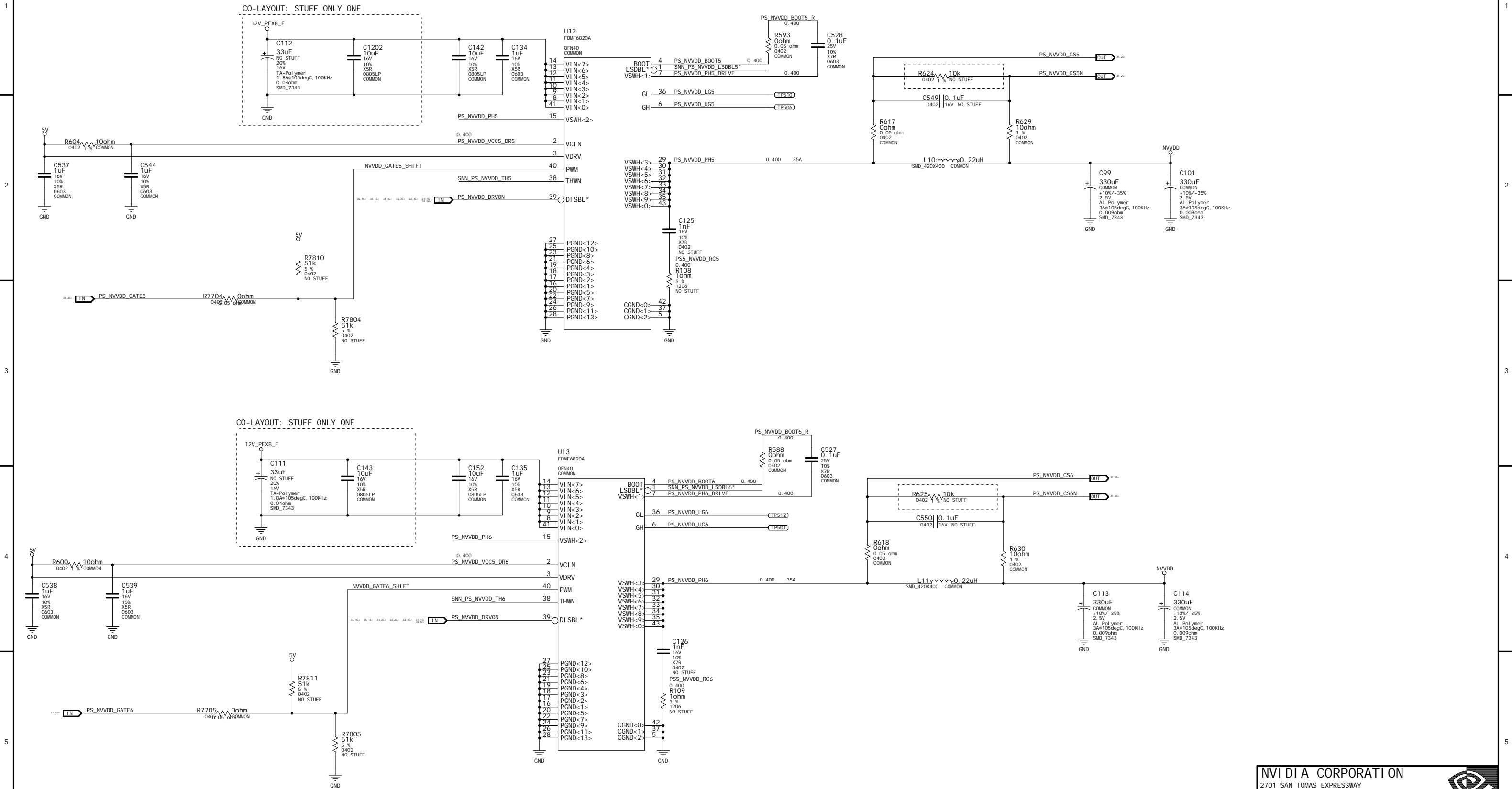
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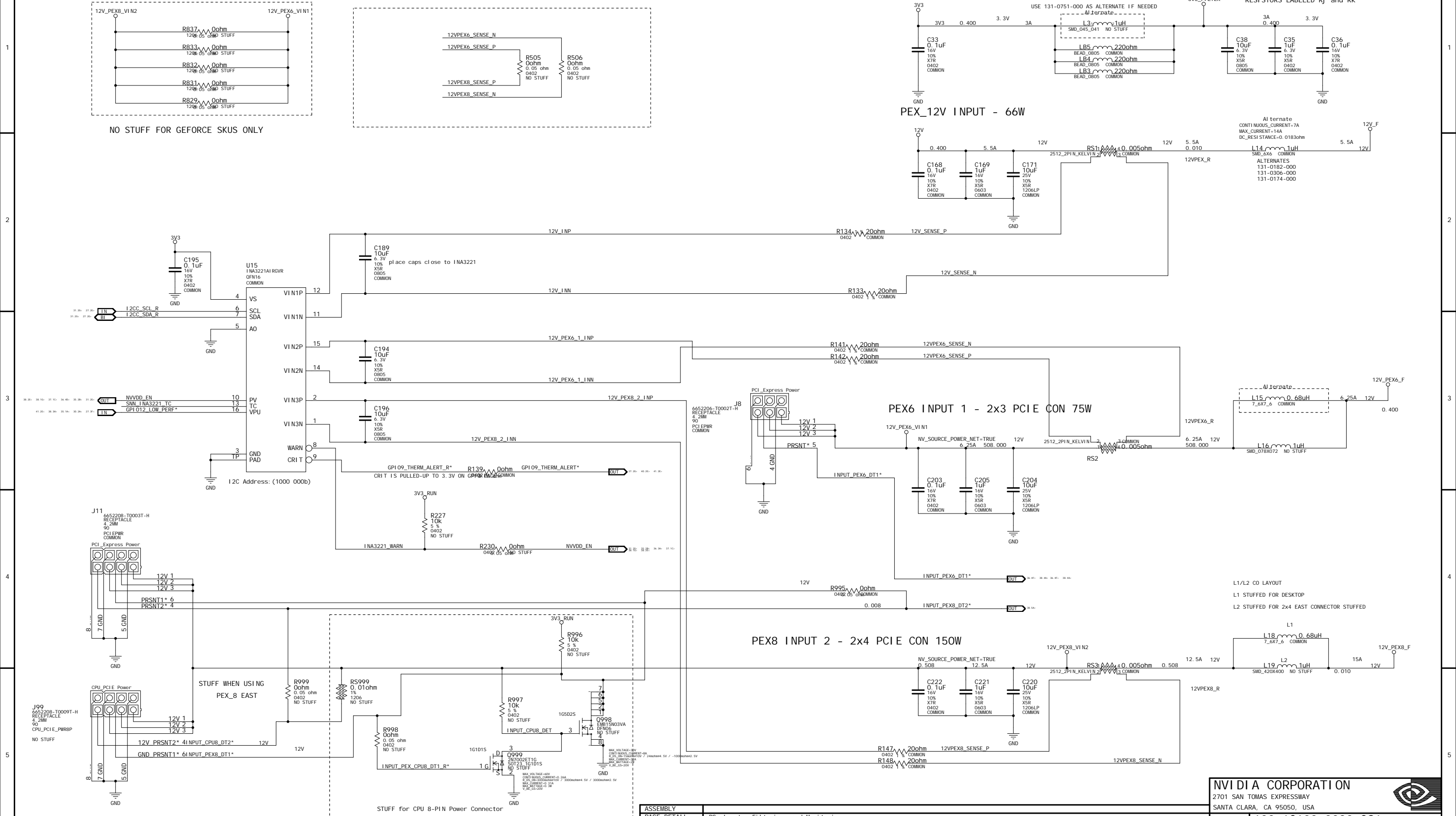
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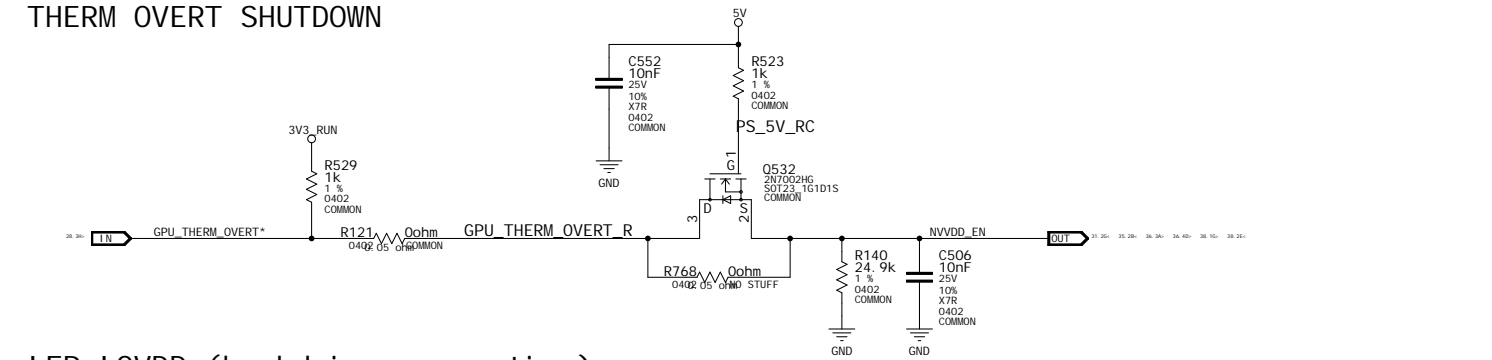
Page36: PS: Inputs, Filtering, and Monitoring



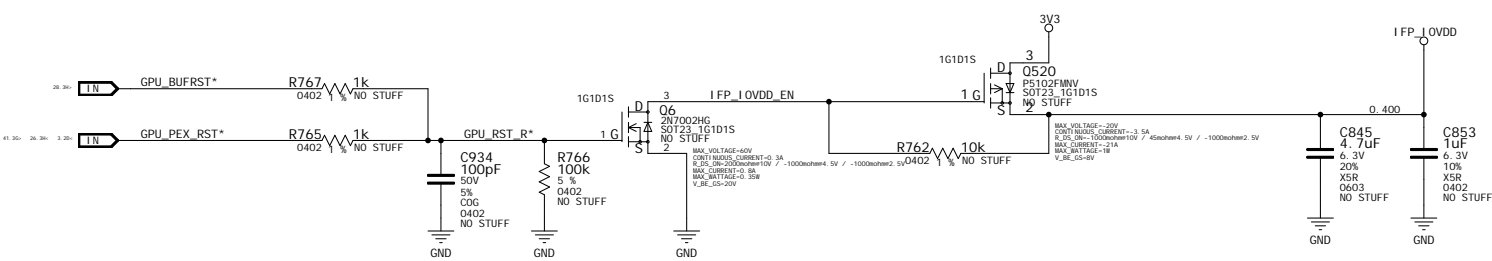
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THERM OVERT SHUTDOWN



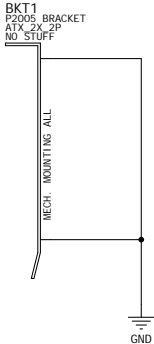
I FP_I OVDD (backdrive prevention)



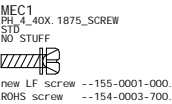
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Brackets:

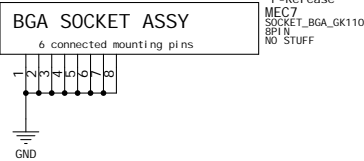
DVI DVI _HDMI _DP : 151-10001-0441-092



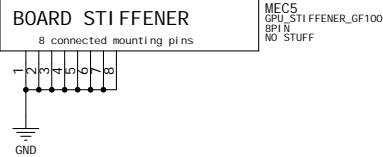
Bracket Screw



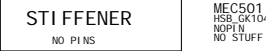
GPU SOCKET



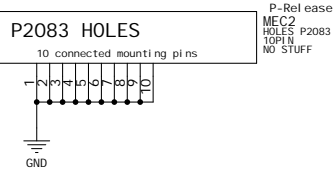
GPU Sti ffener (BRI NG-UP COOLER)



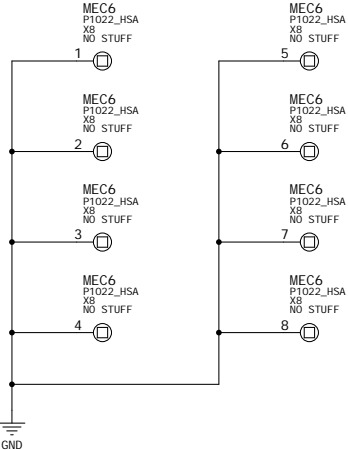
Sti ffener

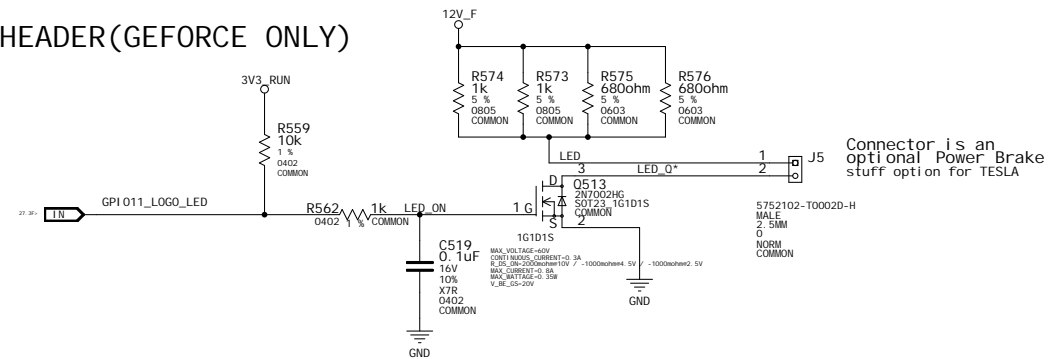


Mechani cal Hol es Symbol



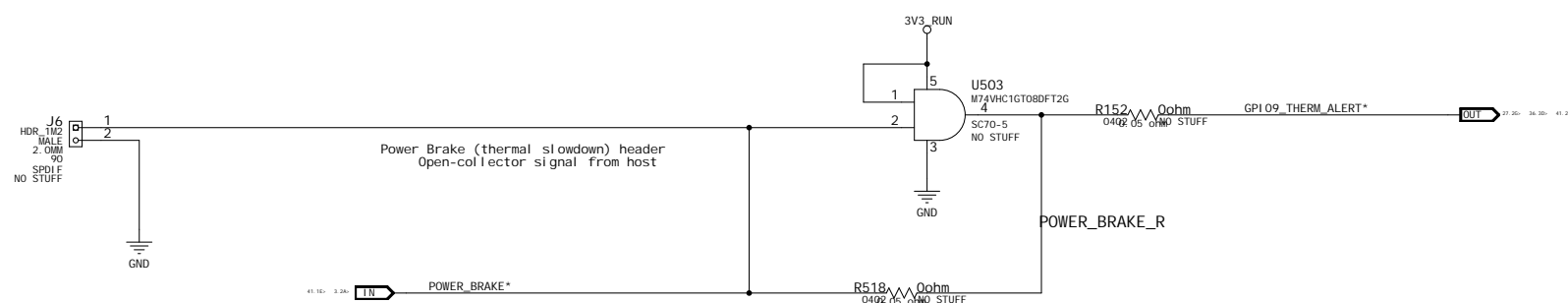
Bri ng Up Cooler



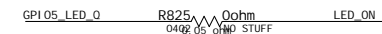


Connector is an optional Power Brake stuff option for TESLA

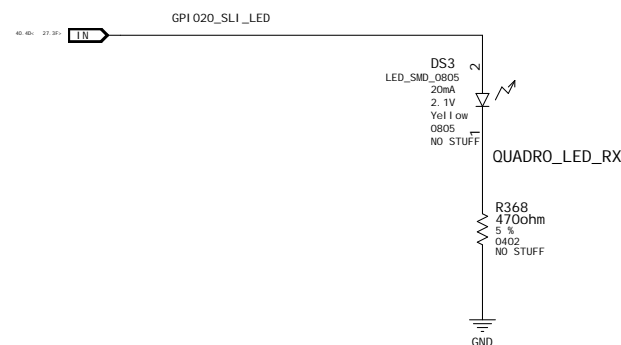
Bypass filter option



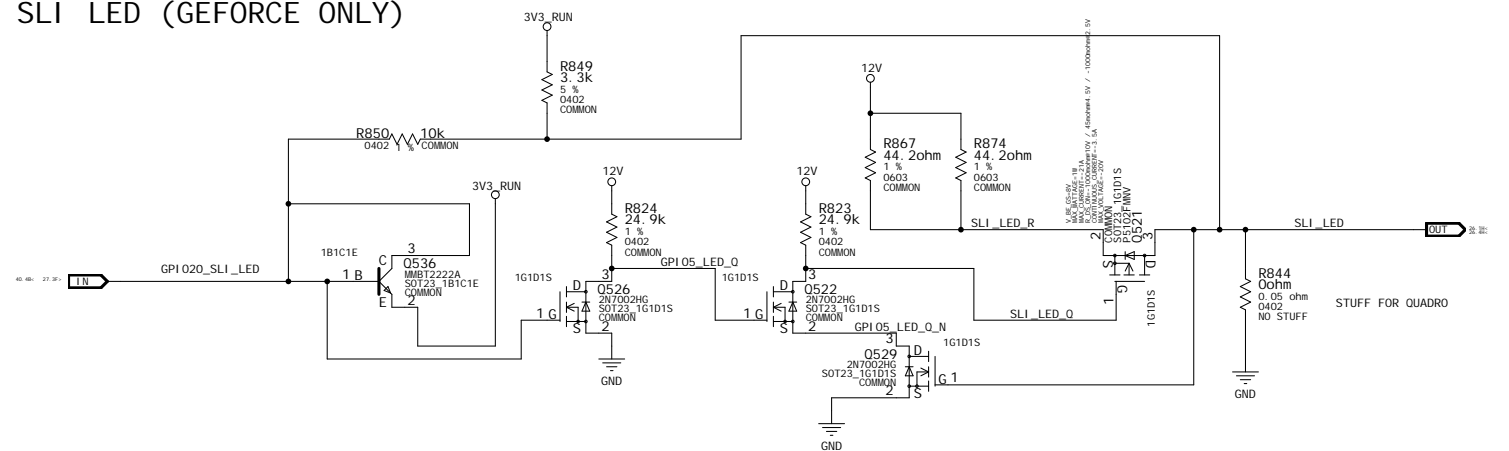
USING GPIO5 TO DIM GEFORCE AND SLI LED



LED FOR QUADRO
PLACE BETWEEN DP Connectors
CONNECTORS



SLI LED (GEFORCE ONLY)



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